



EAST WEST UNIVERSITY

**“Effect of Quantum Mechanical Correction on Drain
Current of Ultra Thin Body SOI MOSFET.”**

By

Mustafa

Said Imam

**In partial fulfillment of the requirements for the degree of
Bachelor of Science in Electrical & Electronic Engineering**

Summer, 2012

Department of Electrical & Electronic Engineering

Faculty of science and engineering

East West University

Effect of Quantum Mechanical Correction on Drain Current of Ultra Thin Body SOI MOSFET.

By

Mustafa

Said Imam

Submitted to the

Department of Electrical & Electronic Engineering

Faculty of science and engineering

East West University

In partial fulfillment of the requirements for the degree of
Bachelor of Science in Electrical & Electronic Engineering

(B.Sc. in EEE)

Summer, 2012

Thesis Advisor
Dr. Anisul Haque

Chairperson
Dr. Mohammad Mojammel Al Hakim

Abstract

Impact of Quantum Mechanical correction in surface potential based compact model on the drain current of UTB SOI MOSFET is studied here. Drain current of FD SOI MOSFET is also observed here. As surface potential based compact model we have selected such a model which incorporate the effect of substrate charge explicitly and it also assumed that the silicon film is always fully depleted and the back silicon film surface is never inverted. We have considered a QM correction model (which is basically used in nanoscale MOSFETs) to the surface potential based compact model of Karim and Haque where the effect of wave function penetration into the gate dielectric is taken into account. In our work we have incorporated the effect of this correction on the drain current characteristics of UTB SOI MOSFET. After the inclusion of QM correction in to the front surface potential (ϕ_{sf}) of UTB SOI MOSFET increase of ϕ_{sf} is observed. Furthermore, QM correction of ϕ_{sf} shows the decrease of drain current of the UTB SOI MOSFET in comparison with the drain current obtain from the semi-classical compact model. For UTB SOI MOSFET, before including QM correction to ϕ_{sf} , a maximum relative error of about 0.6% is obtained between the analytical solution of three surface potentials and iterative solution of exact Poisson equations. In strong inversion, the percentage deviation between saturated drain current of the semi-classical model and quantum corrected model is around 12 – 16%.

Acknowledgement

First of all, we are grateful to the Almighty Allah for giving us this opportunity to complete the research. Then we are grateful to our parents for their incomparable support.

We would like to thank Dr. Anisul Haque, professor, Department of Electrical and Electronic Engineering (EEE), East West University (EWU), Dhaka, our supervisor, for his regular guidance, supervision, constructive suggestions and constant support during this research.

We would also like to thank our former chairperson Dr. Khairul Alam and present chairperson Dr. Mohammad Mojammel Al Hakim, associate professor Department of EEE, EWU, Dhaka.

We also thank to all of our friends and well wishers for their moral support and helpful discussion during this thesis.

Approval

The thesis titled “Effect of Quantum Mechanical Correction on Drain Current of Ultra Thin Body SOI MOSFET” submitted by Mustafa (2008-3-80-011), Said Imam (2009-1-80-048), session summer, 2012, has been accepted satisfactory in partial fulfillment of requirement of the degree of Bachelor of Science in Electrical and Electronic Engineering on August, 2012.

Supervisor

Dr. Anisul Haque

Professor

Department of Electrical and Electronic Engineering,

East West University (EWU),

Dhaka-1212, Bangladesh

Authorization page

We hereby declare that we are the solo author of this thesis. We authorize East West University to lend this thesis to other institution or individuals for the purpose of scholarly research.

Mustafa
(SID: 2008-3-80-011)

Said Imam
(SID: 2009-1-80-048)

We further authorize East West University to reproduce this thesis by photocopy or other means, in total or in part, at the request of other institutions or individuals for the purpose of scholarly research.

Mustafa
(SID: 2008-3-80-011)

Said Imam
(SID: 2009-1-80-048)

Table of Contents

Abstract.....	ii
Acknowledgement	iii
Approval	iv
Authorization page.....	v
Chapter 1.....	1
Introduction.....	1
1.1 Background	1
1.2 Literature Review	2
1.3 Objective	4
1.4 Organization of the thesis.....	4
Chapter 2.....	5
Surface Potential Based Model for FD SOI MOSFET	5
2.1 Appreciation of the Surface Potential Based Model	5
2.2 Introduction to Fully Depleted SOI structure.....	6
2.3 Effect of substrate charge on the Surface Potential.....	6
2.4 Analytical Solution of Surface Potential	8
2.4.1 SURFACE POTENTIAL SOLUTION:	10
2.4.2 Weak inversion:	10
2.4.3 Strong Inversion:.....	12
2.4.4 Single piece model.....	13
2.5 Surface Potential based drain current model.....	13
Chapter 3.....	15
Quantum Mechanical Effect	15
3.1 Energy quantization in the Silicon film due to quantum mechanical effects.....	15
3.1.1 Threshold Voltage shift.....	16
3.1.2 Shift in surface potential	16
3.2 Quantum Mechanical Correction to the Surface Potential of Nanoscale FD SOI MOSFETs.....	17
3.2.1 Basic approach of the Karim and Haque QM model.....	17
3.2.2 Derivation of a mathematical expression of the proposed QM model	19
Chapter 4.....	21
Results and Discussion	21
4.1 Surface Potential	21
4.2 Drain Current.....	25
Chapter 5.....	28
Summary.....	28

5.1	Conclusion.....	28
5.2	Future Work	28
	Appendix.....	30
	References.....	37

List of Figures

Figure 2.1:	Energy Band Diagram for Depletion mode.....	5
Figure 2.2:	Cross-sectional view of the FD SOI MOSFET.....	7
Figure 2.3:	Substrate surface potential ϕ_{sbulk} versus gate voltage for different substrate doping.	7
Figure 2.4:	Electric field shape from the Si/SiO ₂ interface of the front gate oxide toward the substrate. The solid lines specify the electric field distribution for a given gate voltage. The dashed lines express the electric field when the silicon film is just depleted.....	9
Figure 2.5:	Surface potential vs Gate voltage.....	11
Figure 3.1:	Discrete energy levels due to quantization (in the substrate).....	15
Figure 3.2:	Electron concentration distribution in the silicon substrate in classical and quantum mechanical cases.....	16
Figure 4.1:	For FD SOI, comparison of ϕ_{sf} obtained iteratively and analytically. Here, $t_{\text{soi}} = 25$ nm and $t_{\text{box}} = 50$ nm.	22
Figure 4.2:	For FD SOI, $\phi_{\text{sf,weak}}$, $\phi_{\text{sf,strong}}$, and $\phi_{\text{sf,iterative}}$ versus gate voltage. Here, $t_{\text{soi}} = 25$ nm and $t_{\text{box}} = 50$ nm.....	23
Figure 4.3:	For FD SOI, three surface potentials ϕ_{sf} , ϕ_{sb} , and ϕ_{sbulk} versus gate voltage. Here, $t_{\text{soi}} = 25$ nm and $t_{\text{box}} = 50$ nm.	23
Figure 4.4:	For FD SOI, ϕ_{sf} versus gate voltage for different values of V_{CB} . Here, $t_{\text{soi}} = 25$ nm and $t_{\text{box}} = 50$ nm.....	24
Figure 4.5:	For UTB SOI, ϕ_{sf} versus gate voltage for different values of V_{CB} with QM correction. Here, $t_{\text{soi}} = 8$ nm and $t_{\text{box}} = 50$ nm.	25
Figure 4.6:	For FD SOI, V_{DS} versus I_{DS} for different V_{GS} . Here, $t_{\text{soi}} = 25$ nm and $t_{\text{box}} = 50$ nm.	26
Figure 4.7:	For UTB SOI, V_{DS} versus I_{DS} for different V_{GS} including QM correction of Drain current. Here, $t_{\text{soi}} = 8$ nm and $t_{\text{box}} = 50$ nm.	26

List of Table

Table 4.1:	Parameter used in surface potential model verification.....	21
Table 4.2:	Percentage difference of Saturation Current.....	27
Table 4.3:	Difference of V_{DS} for obtaining transition point	27

Chapter 1

Introduction

The modern era of semiconductor electronics was guided by the invention of the bipolar junction transistor in 1948. In the 1960s MOS transistor technology has been introduced. Since then significant development of the MOS transistor technology has been done. Also dimensions of the transistors have decreased regularly. Currently bulk MOSFETs are reaching to the saturation of the scaling process. SOI MOSFET has been introduced in this process of the MOS transistor technology development. UTB SOI MOSFET is the successor of SOI MOSFET.

A SOI MOSFET is Silicon on Insulator (SOI) structure in which a semiconductor layer, like silicon is formed above an insulator layer. The SOI technology is introduced to overcome the limits of bulk or conventional Si MOSFETs. As MOSFETs goes to the nanometer region, SOI MOSFETs come with ultra thin body (UTB) where silicon film thickness is a few nanometers. As a result semi-classical mechanics does not exactly explain the performance of the UTB devices. In this situation Quantum Mechanical (QM) effects have started to play vital role in terms of performance of the UTB SOI MOSFET. Earlier QM effect was neglected because of the larger device size. Therefore it is necessary to include QM effects in transistor models.

In this work, we have analyzed QM effect over the front surface potential of the UTB SOI MOSFETs. Quantum mechanical effect on the drain current due to ultra thin body of SOI structure has been incorporated using a compact model. Usually compact models are the circuit models describing the terminal properties of the semiconductor devices that can be employed in circuit simulators. The properties of the devices in compact models are either defined by means of a simplified set of equations or by an equivalent circuit model. Results are presented and discussed.

1.1 Background

Among the non-classic CMOS device concepts, an UTB SOI is one of the most promising approaches for future CMOS scaling to feature sizes below 50 nm. In contrast to other emerging device concepts, the UTB SOI technology combines a planar transistor configuration with a superior sub-threshold slope resulting from a thin Si-body thickness of 5–40 nm [1]. Together with reduced junction capacitances, high-k dielectrics, poly-SiGe gates or metal gates, these are attractive features for an energy-efficient CMOS logic operated at low supply voltages. With continual scaling of CMOS technology classical physics is inadequate to explain the behavior of a UTB SOI MOSFET. For modern day physics, where the MOS devices are down-scaled to the nanometer regime, QM effects have become an essential part [2].

To keep pace with the high density integration for SOI devices, it is necessary to reduce the silicon film thickness. This results in a narrow and deep potential well in the channel. Electrons get confined at the semiconductor-insulator interface and it becomes necessary to take QM effects into consideration. In the state-of-the-art devices due to increased vertical electrical field the carrier energy quantization has become significant. The energy quantization, threshold voltage (V_{th}) shift and increase in surface potential are the results of the QM effect.

In order to predict the device performance and QM effect precisely various models have been developed, such as, numerical device simulation models, compact models etc. The requirements of numerical models, such as, rigorous computation and huge amount of memory, prevent them from being used for circuit simulation. Terminal properties of the devices have been described by the compact models by using simplified computation or by an equivalent circuit model. So these compact models are very popular for circuit simulation. QM effect can be predicted or modeled easily by compact models.

1.2 Literature Review

The generation of the idea of building MOSFET on an insulator was started at 1960s, and the idea was first applied in the thin-film transistor (TFT). At 1964 the first SOI transistors was implemented, which was a partially depleted device, fabricated on silicon-on-sapphire (SOS) substrates [3]. A variety of short-channel effects become significant as the scaling of CMOS technology continues to move into nanometre regime for high density and high performance integrated circuits, which limit the scaling of the device. In that situation, multi-gate MOSFET devices seem to be more attractive to control this limitation. Recently, excellent electrical characteristics have been shown by various transistors fabricated with a double gate structure. Moreover fully depleted (FD) SOI with ultra-thin body appeared to be the first device to replace the classical MOS architecture [4]. Compact models for SOI-MOSFETs have been developed by different research groups.

A number of analytical models have been suggested in the literature for modeling the current-voltage characteristics and the surface potential of SOI MOSFET, starting from the one-dimensional threshold voltage analytical model for thin film SOI MOSFETs, published by Lim and Fossum in 1983 [5]. Another model, which evaluates the surface potential for both partially depleted (PD) and FD SOI MOSFETs, using a single unified expression, proposed by Yu et al. [6] and the model is simplified one-dimensional analytical model. The model is free of iterations which is an advantage of this model [6] unlike the surface potential models given by Sleight and Rios [7] and by Bolouki et al. [8]. However, there are some weak points in the model given by Yu et al. [6] like, inability to correctly model the dependence of the front surface potential on the substrate voltage, self-inconsistent results due to misrepresentation of the operating modes of SOI devices, and ignoring the contribution of the inversion charge while expressing the back surface potential of the SOI film [9]. One of the advantages of this model [6] is that it provides a single formula for the

drain current which is obtained by smoothly connecting the analytic solutions for various operating regions.

Surface potential based MOSFET models have emerged as a better replacement to the threshold voltage based models. One of the main cause is surface potential based models provide consistent and accurate expressions for terminal currents and charges. These expressions are also valid in all regions of operations [10]–[17]. Many models based on surface potential approach have been developed for bulk MOSFETs which were implemented in different circuit simulators [11]–[14]. Surface potential based compact models have become popular for sub 100nm MOSFETs. However, modeling of FD SOI MOSFET is not same as MOSFETs because depletion charge in the substrate region is appear in FD SOI. FD SOI models like [6], [18], [19] do not consider the substrate depletion which were reported between 1989 to 2005 and because of this, these models cannot be used for FD SOI devices which have low substrate doping. Surface potential based FD SOI model of “Hiroshima University Semiconductor Technology Academic Research Centre IGFET model SOI (HiSIM-SOI)” [19] considers the substrate depletion explicitly.

The model of Francis et al. [20] has estimated the depletion charge by a constant value which is no longer valid in strong inversion regime for doped DG SOI transistors. As a result the model becomes less accurate in strong inversion. Some authors [21], [22], have presented a surface potential model for doped FD SOI MOSFETs. On the other hand, FD SOI model of HSiM [20] did not make any assumption, but the weak point of this model is that a single equation is provided to compute three different surface potentials (front, back and bulk surface potentials) that make the model inefficient. Unlike HSiM, recently published model [22] presented three equations for the three different surface potentials of the device.

To describe the transition characteristics between partially depleted and fully depleted operating regimes, a few compact models for SOI MOSFETs have been reported [7], [22], [23], [24]. The continuous compact model [7] is naturally continuous for the transition between the FD region and the PD region and uses an iterative procedure to calculate the front surface potential. In this model [7] the one-dimensional (1-D) Poisson equation was used to calculate the surface potential. But, in a large-scale simulation, the iteration could be a burden. The quasi-two-dimensional unified analytical front surface potential model [23] can explain both the FD region and the PD region. Although [23] is a fully analytic model, an iteration routine is required to obtain the critical front gate voltage defining the PD region and the FD region. The quasi-2-D nature of the model results in a surface potential in the strong inversion region and in the accumulation region that is different from the numerical solution of the 1-D Poisson equation. On the other hand BSIM SOI [24] is totally different from the surface potential models and uses an explicit threshold. The model most widely applied by industries is BSIM SOI based on the threshold-voltage concept [25]. By introducing an internal node this model [25] solves an unavoidable floating-body effect and the node potential is described analytically as a function of applied biases.

Circuit-simulation models for the SOI MOSFET have been developed to enable a reliable circuit design. Berkeley short-channel IGFET model-SOI (BSIM SOI) [26] and University of Florida SOI (UFSOI) [27], [28], are two major existing models which have been applied for the practical circuit simulation. Both models considered smooth transition between the partially depletion and the fully depletion condition during circuit operation.

There are some important features such as the parasitic bipolar effect and the generation-recombination current which have been included in those models [26]-[28]. These features are specific for the SOI-MOSFET. Both models have been developed as an extension of the bulk-MOSFET and suffer from nonconvergence problems in the circuit simulation [29], [30].

Now, it becomes important to have a closed-form single-equation solution of surface potential for different surfaces of the FD SOI device so that it can be used in circuit simulators. There is such solution available in the [22] that solves surface potentials at all surfaces of the FD SOI MOSFET explicitly considering the effect of substrate depletion. Here, by solving the 1-D Poisson equation a closed-form surface potential solution has been reported for all the surfaces of fully depleted SOI MOSFETs.

All the above models are based on semi-classical analysis. Several models have been proposed to incorporate QM effect in the surface potential of the bulk MOSFETs. Most exciting models incorporate QM correction through the band gap widening approach [31]. In 2010, a different QM correction approach to the semi-classical surface potential was proposed [32]. It directly adds the QM correction term to semi-classical surface potential. The model accounts for effect of wave function penetration within the proposed correction. This model proposed an explicit analytical term, $\delta\phi_{sf}$, which has been directly added to the semi-classical surface potential. $\delta\phi_{sf}$ is the quantum mechanical correction to the semi-classical front surface potential.

1.3 Objective

First of all our aim is to analyze the behavior of three surface potentials of the FD SOI MOSFETs, namely front oxide-silicon film surface ϕ_{sf} , buried oxide-silicon film interface ϕ_{sb} , and buried oxide-substrate interface ϕ_{sbulk} due to the applied gate voltage. Also our objective is to analyze the drain current of FD SOI MOSFETs.

On the other hand in order to understand how the performance of UTB SOI MOSFET is affected by quantum mechanical effects, it is necessary to incorporate the QM correction on the semi-classical surface potential based compact model. The Karim and Haque model of [32] is a physically based model for QM corrections to the MOS surface potential. So our objective is to incorporate the QM effect into the surface potential of the UTB SOI MOSFET by using this model. We also want to investigate how QM effect influence the drain current of the UTB SOI MOSFET.

1.4 Organization of the thesis

In chapter 2 necessary reviews of SOI MOSFET and drain current model are discussed. In the following chapter 3, a brief explanation on QM effects and their theoretical derivation are given. Then later in chapter 3, basic approach of Karim and Haque model and mathematical derivations are explained. In chapter 4 and chapter 5, summary of results of the whole work, and conclusion, proposed work for the future are given respectively.

Chapter 2

Surface Potential Based Model for FD SOI MOSFET

Surface potential is the total potential drop across the semiconductor region from the surface to a point in the bulk. In other word surface potential is the potential difference across the space charge layer. According to the SOI literatures there are three surfaces for the FD SOI MOSFET, these exist at front oxide–silicon film interface, buried oxide–silicon film interface, and buried oxide–substrate interface. The potentials at these Si/SiO₂ interfaces are functions of the terminal voltages as shown in Figure 2.1.

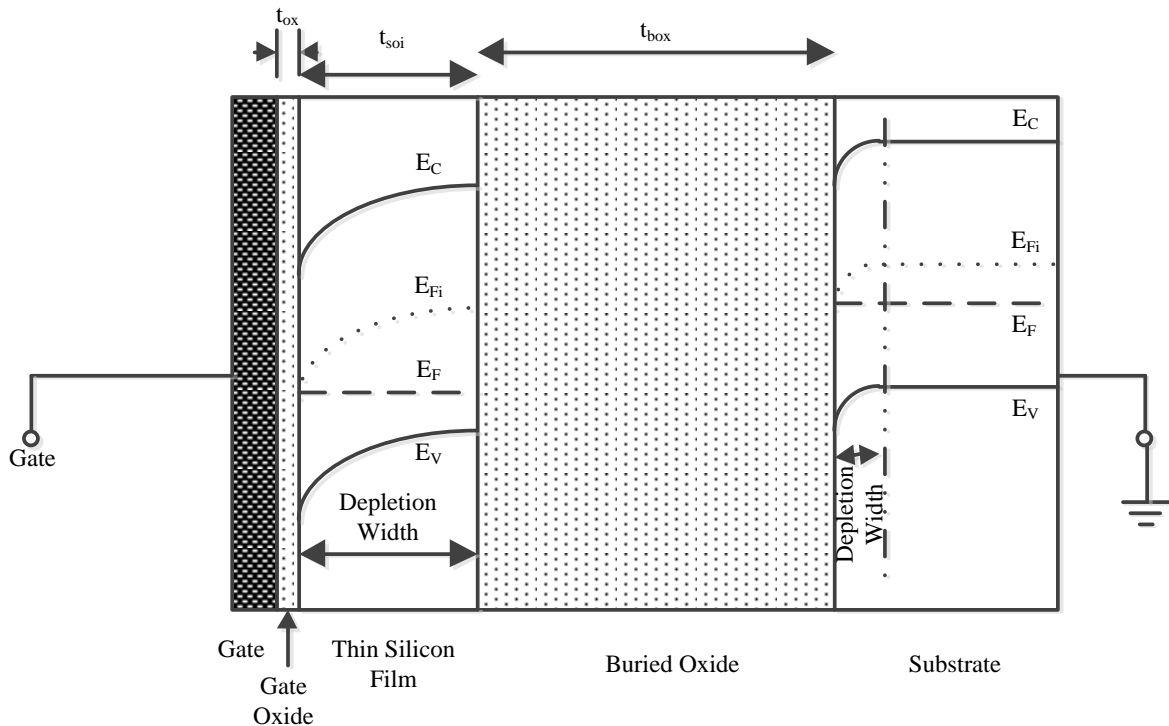


Figure 2.1: Energy Band Diagram for Depletion mode.

2.1 Appreciation of the Surface Potential Based Model

In case of designing compact model the surface potential based model enhances the physical content and makes it more suitable for modeling advanced MOS devices. For getting consistent and accurate expressions for terminal currents and charges (which is valid in all regions of operations) surface potential based MOSFET models provide best results. Prior to surface potential based model the threshold voltage based models were used. As surface potential based models are suitable for simulating circuits with low power supply voltages and also allow physical modeling of the subthreshold region, which were the main drawbacks of the threshold-voltage-based models. Surface potential based models are better alternative to the threshold voltage based models [33]. Based on surface potential approach many models

have been developed for bulk MOSFETs and implemented in different circuit simulators. The same modeling approach has been extended to PDSOI MOSFET with a special consideration to effects, specific to PDSOI MOSFET, such as floating body and self-heating effects [34], [35]. Due to appearance of depletion charge in the substrate region, modeling of FD SOI MOSFET is quite different than bulk MOSFET. As a result, the surface potential based approach provides substantial advantage in the improvement of compact models. It also allows one to increase the physics content of the model. Furthermore, surface potential is a physical variable, which is a single expression for a particular surface.

2.2 Introduction to Fully Depleted SOI structure

In case of an NMOS transistor, applying a positive gate voltage depletes the body of P-type carriers and induces an N-type inversion channel on the surface of the body. For SOI structure a thin Silicon film is sandwiched between two oxide layers (i.e. Gate oxide and Buried oxide). As the film gets thinner the floating voltage becomes negligible. The two basic versions of single gate (SG) SOI MOSFET are the partially depleted (PD) SOI architecture and fully depleted (FD) SOI architecture. For PDSOI the silicon layer thickness is greater than the depletion layer, and for FDSOI the depth of the silicon layer thickness is equal to the thickness of the depletion region under the gate [36]. Figure 2.2 shows a fully depleted SOI MOSFET structure. The doping and the thickness for this type of SOI are varied in such a way that the SOI is fully depleted when the channel is inverted. As mentioned earlier the maximum depletion width for this type of SOI is equal to the thickness of the SOI film.

2.3 Effect of substrate charge on the Surface Potential

In case of FD SOI the threshold voltage depends not only on the metal oxide work function, Fermi potential, and gate oxide fixed charge but also on the potential of the back channel. This back channel potential evolved from substrate charge. If the potential of the back channel is varied in such a way that it follows the potential of the front channel, then the threshold voltage will be smaller than that of the bulk MOSFET and the sub-threshold slope will be close to ideal value.

To further highlight the effect of substrate charge, plot of ϕ_{sbulk} for different values of substrate doping is given in Figure 2.3. When the substrate doping is small (e.g., 10^{15} cm^{-3}), then a large voltage drop appears across the substrate depletion region. With the increase of substrate doping, decrease of voltage drop across the substrate depletion region is observed.

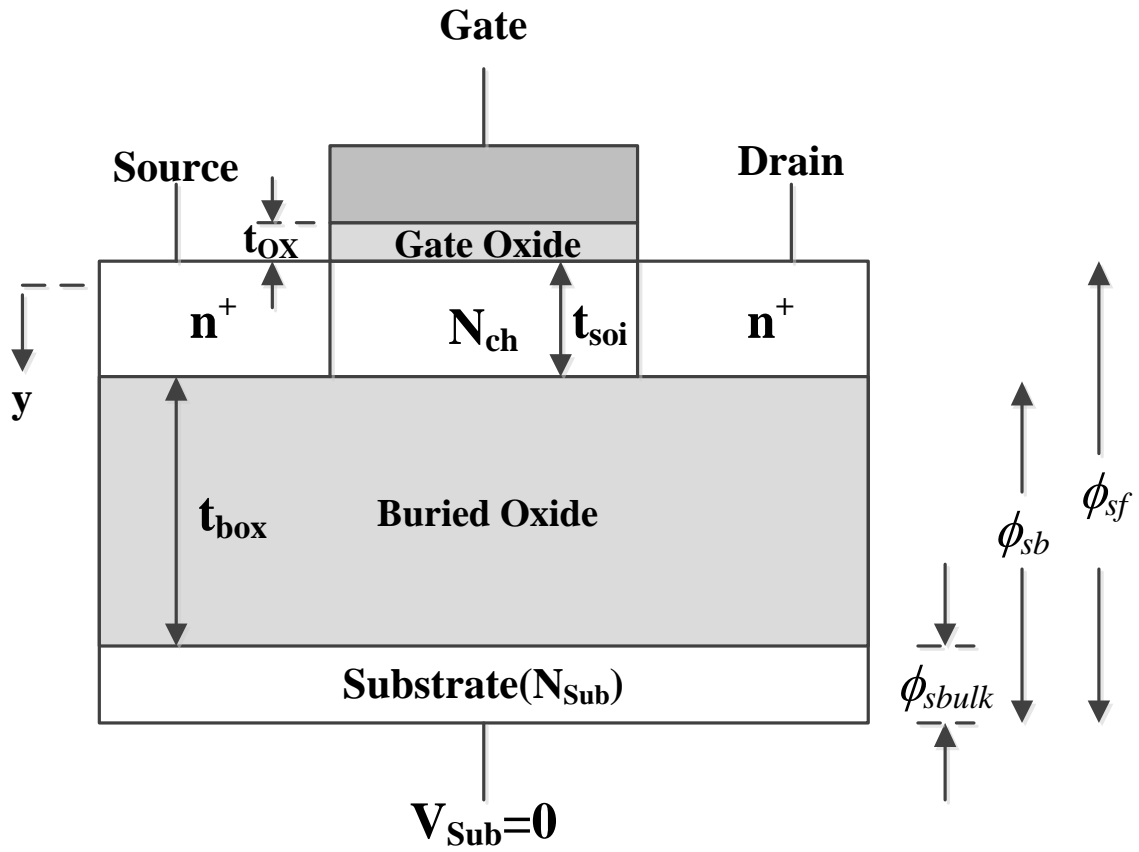


Figure 2.2: Cross-sectional view of the FD SOI MOSFET.

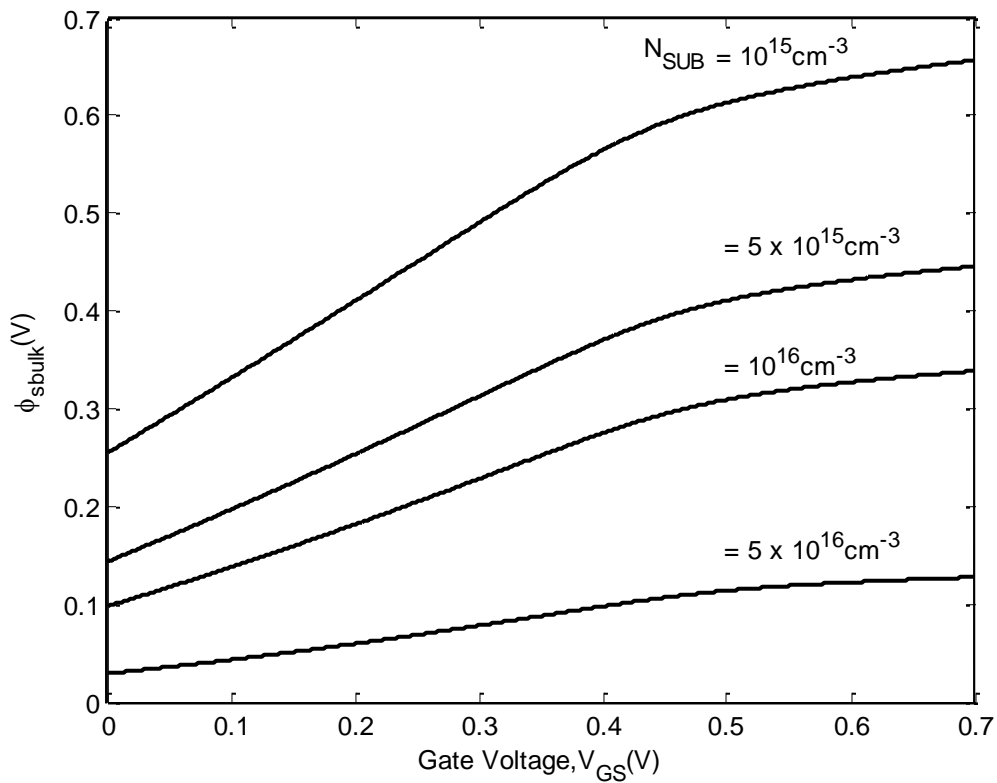


Figure 2.3: Substrate surface potential ϕ_{sbulk} versus gate voltage for different substrate doping.

2.4 Analytical Solution of Surface Potential

Two assumptions are primarily taken for getting analytical solution of surface potentials (namely front oxide–silicon film surface ϕ_{sf} , buried oxide–silicon film interface ϕ_{sb} , and buried oxide–substrate interface ϕ_{sbulk}) for FD SOI MOSFET. These are: 1) The silicon film is always fully depleted and 2) The back silicon film surface is never inverted. By solving the 1-D Poisson equation in vertical direction and applying the boundary conditions at different surfaces three different equations are obtained [22].

In case of a FD SOI MOSFET as shown in Figure 2.2, the 1-D Poisson equation can be written as

$$\frac{\partial^2 \phi(y)}{\partial y^2} = -\frac{q}{\epsilon_{Si}} (p(y) - n(y) - N_{ch}) \quad (2.1)$$

where $\phi(y)$ is the potential, ϵ_{Si} is the permittivity of silicon, $p(y)$ and $n(y)$ are the hole and electron concentrations, respectively and N_{ch} is the doping in the silicon layer [22].

By expanding the parentheses of (2.1) it can be further expressed as

$$\frac{\partial^2 \phi(y)}{\partial y^2} = -\frac{qN_{ch}}{\epsilon_{Si}} \left\{ \left[\exp\left(-\frac{\phi(y)}{\phi_t}\right) - 1 \right] - \exp\left(-\frac{2\phi_F + V_{CB}}{\phi_t}\right) \left[\exp\left(\frac{\phi(y)}{\phi_t}\right) - 1 \right] \right\} \quad (2.2)$$

where ϕ_F is the Fermi potential, ϕ_t is the thermal voltage, and V_{CB} is the channel floating body potential, which varies from V_{SB} at source to $V_{SB} + V_{DS}$ at drain [22].

The boundary conditions need to be used in (2.2) are as follows:

- 1) Electric flux (displacement) at the front oxide/Si film interface is continuous (Gauss Law).

$$-\frac{\partial \phi(y)}{\partial y} \Big|_{\phi(y)=\phi_{sf}} = \left(\frac{V_g - \phi_{sf}}{t_{ox}} \right) \frac{\epsilon_{ox}}{\epsilon_{Si}} \quad (2.3)$$

where ϵ_{ox} is the permittivity of the gate oxide, t_{ox} is the thickness of front gate oxide, and $V_g = V_{GS} - V_{FB}$, where V_{GS} is the gate-to-source bias voltage and V_{FB} is the flat-band voltage.

- 2) Electric flux at the buried oxide/Si film interface is continuous (Gauss Law).

$$-\frac{\partial \phi(y)}{\partial y} \Big|_{\phi(y)=\phi_{sb}} = \left(\frac{\phi_{sb} - \phi_{sbulk}}{t_{box}} \right) \frac{\epsilon_{ox}}{\epsilon_{Si}} \quad (2.4)$$

where t_{box} is the thickness of buried oxide, ϕ_{sb} is the surface potential at the buried oxide–silicon film interface, and ϕ_{sbulk} is the surface potential at the buried oxide–substrate interface [22].

Substituting the two aforementioned boundary conditions the following equation is obtained.

$$\left(V_g - \phi_{sf} \right)^2 - \frac{C_{box}^2}{C_{ox}^2} (\phi_{sbulk} - \phi_{sb})^2 = -\gamma^2 \left\{ \begin{array}{l} -\phi_t \left[\exp\left(-\frac{\phi_{sf}}{\phi_t}\right) - \exp\left(-\frac{\phi_{sb}}{\phi_t}\right) \right] - (\phi_{sf} - \phi_{sb}) \\ -\exp\left(-\frac{2\phi_F + V_{CB}}{\phi_t}\right) \left(\phi_t \left[\exp\left(\frac{\phi_{sf}}{\phi_t}\right) - \exp\left(\frac{\phi_{sb}}{\phi_t}\right) \right] \right) \\ -(\phi_{sf} - \phi_{sb}) \end{array} \right\} \quad (2.5)$$

where $\gamma = \frac{\sqrt{2qN_{ch}\epsilon_{si}}}{C_{ox}}$ and $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ And $C_{box} = \frac{\epsilon_{box}}{t_{box}}$

Equation (2.5) has three unknowns namely ϕ_{sf} , ϕ_{sb} and ϕ_{sbulk} . It is known from mathematics that, to solve three unknowns three equations are needed. Therefore, two more equations are required to solve the unknowns and they can be obtained by solving the Poisson equation in the silicon film layer and the substrate region [22].

The Poisson equations for the substrate and silicon film are given by (2.6) and (2.7), respectively by assuming that inversion at the back silicon film surface and substrate never happen.

$$\frac{\partial^2 \phi(y)}{\partial y^2} = -\frac{1}{\epsilon_{Si}} (-qN_{sub}) \quad (2.6)$$

$$\frac{\partial^2 \phi(y)}{\partial y^2} = -\frac{1}{\epsilon_{Si}} (-qN_{ch}) \quad (2.7)$$

In case of writing (2.7) small voltage drop appearing across the front surface inversion charge layer has ignored, which simplifies the equation.

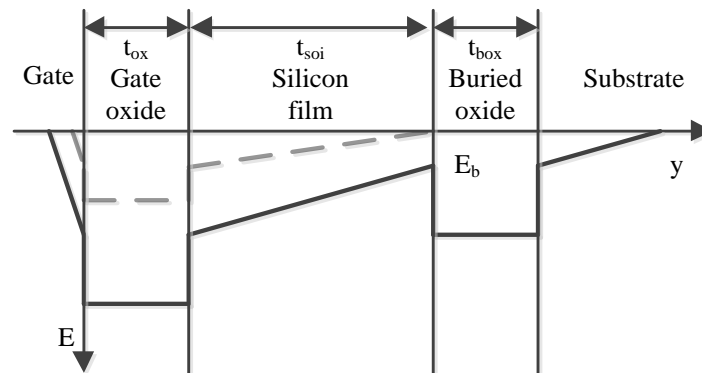


Figure 2.4: Electric field shape from the Si/SiO₂ interface of the front gate oxide toward the substrate. The solid lines specify the electric field distribution for a given gate voltage. The dashed lines express the electric field when the silicon film is just depleted.

Solving Poisson's equation (2.6) and (2.7) following equations are obtained

$$\phi_{sf} - \phi_{sb} = \alpha + (\phi_{sb} - \phi_{sbulk}) \frac{C_{box}}{C_{soi}} \quad (2.8)$$

$$\phi_{sb} = \phi_{sbulk} + \gamma_{bulk} \sqrt{\phi_{sbulk}} \quad (2.9)$$

where $\gamma_{bulk} = \frac{\sqrt{2qN_{sub}\epsilon_{si}}}{C_{box}}$, $\alpha = \frac{qN_{ch}t_{soi}^2}{2\epsilon_{si}}$, $C_{soi} = \frac{\epsilon_{ox}}{t_{soi}}$, and $C_{box} = \frac{\epsilon_{ox}}{t_{box}}$

(2.5), (2.8) and (2.9) together describe the exact Poisson equation for an FD SOI MOSFET and are obtained without any approximation except the assumptions that the back silicon surface and the substrate region never go into inversion and that the device always remains in FD condition. By solving (2.5), (2.8) and (2.9) iteratively one can get the exact values of all three surface potential expressions [22].

Due to the nonlinear nature of (2.5), (2.8) and (2.9) a single closed-form solution for the surface potential cannot be obtained for the FD-SOI MOSFET as in the case of bulk MOSFETs. Therefore, separate solutions are first obtained in the weak and strong inversion regions, later; they are merged to get a single closed-form expression, as discussed in the following sections.

2.4.1 SURFACE POTENTIAL SOLUTION:

To obtain the single closed-form solution for the surface potential, it is further assumed that the MOSFET does not operate in the accumulation region, which is a quite a valid assumption as the accumulation region is rarely used except in some specific applications. Hence, when $\phi_{sf} > 3\phi_t$, (2.5) becomes

$$\begin{aligned} & \frac{1}{\gamma^2} \left((V_g - \phi_{sf})^2 - \frac{C_{box}^2}{C_{ox}^2} (\phi_{sbulk} - \phi_{sb})^2 \right) \\ & = (\phi_{sf} - \phi_{sb}) + \phi_t \left(1 - \exp\left(-\frac{\phi_{sf} - \phi_{sb}}{\phi_t}\right) \right) \times \exp\left(\frac{-2\phi_F - V_{CB} + \phi_t}{\phi_t}\right) \end{aligned} \quad (2.10)$$

Finally, (2.8)–(2.10) are solved for the weak and strong inversion cases so that they can be unified with the help of smoothing functions as in the case of the bulk MOSFET.

2.4.2 Weak inversion:

It is observed from Figure 2.5 that when $\phi_F < \phi_{sf} < \phi_{2F}$ the MOSFET operates in weak inversion region. In this region, the small inversion charge appearing at the front silicon film surface can be neglected, as in the case of the bulk MOSFET. When the MOSFET is operating in weak inversion, the electric field variation in the vertical direction is shown in Figure 2.4, where the solid line denotes the electric field at a certain gate voltage V_{GS} . In this case V_C is the minimum voltage necessary to keep the device in the FD mode. In Figure 2.4,

the dotted line denotes the electric field variation in the vertical direction at V_C . At this voltage, the electric field at the buried oxide–silicon film interface becomes zero. Therefore, V_C can be written as

$$V_C = \alpha + \frac{qN_{Ch} t_{soi}}{C_{ox}} \quad (2.11)$$

Voltage $V_g (=V_{GS} - V_{FB})$ is equivalent to the entire area under the electric field curve, shown in Figure 2.4.

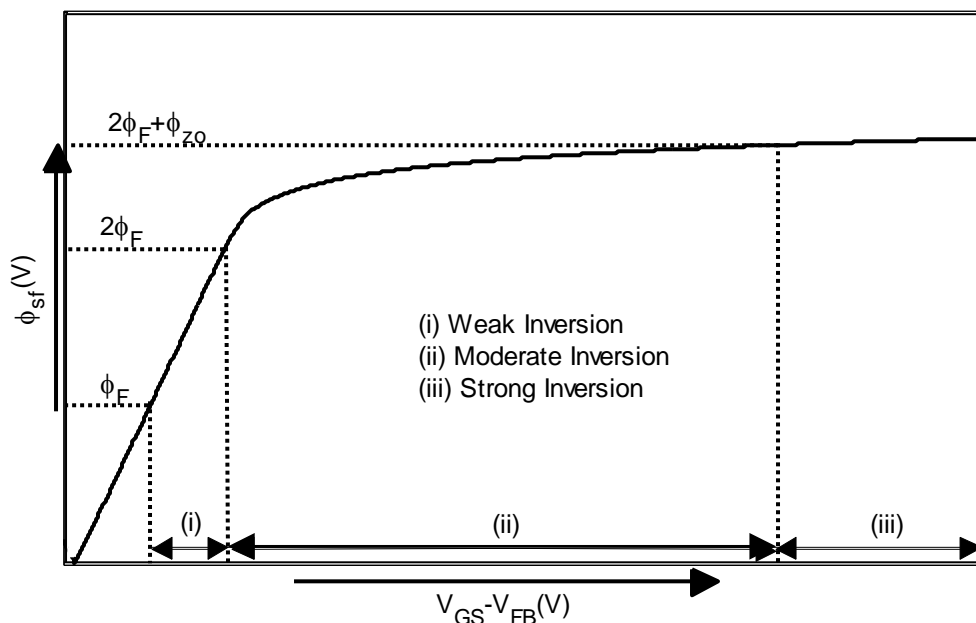


Figure 2.5: Surface potential vs Gate voltage.

E_b is the electric field at the buried oxide/substrate interface when the device has just reached FD. E_b can be written with respect to V_g as

$$E_b = -\frac{qN_{sub}}{C_{eff}} + \sqrt{\left(\frac{qN_{sub}}{C_{eff}}\right)^2 + \frac{2qN_{sub}}{\epsilon_{Si}}(V_g - V_C)} \quad (2.12)$$

where $\frac{1}{C_{eff}} = \frac{1}{C_{ox}} + \frac{1}{C_{box}} + \frac{1}{C_{soi}}$ and N_{sub} is the substrate doping.

Finally, the value of E_b is used to obtain the expression of front surface potential in weak inversion as

$$\phi_{sf,weak} = V_g - \frac{\epsilon_{Si} t_{ox}}{\epsilon_{ox}} \left(E_b + \frac{qN_{ch} t_{soi}}{\epsilon_{Si}} \right) \quad (2.13)$$

where $\phi_{sf,weak}$ denote the front surface potential in the weak inversion region.

2.4.3 Strong Inversion:

In the strong inversion region, (2.10) can be rearranged as (2.14).

$$\phi_{sf, strong} = 2\phi_F + V_{CB} + \phi_t \ln \left(\frac{\frac{1}{\gamma^2} (V_g - \phi_{sf, strong})^2 - \frac{C_{box}^2}{C_{ox}^2} (\phi_{sbulk, strong} - \phi_{sb, strong})^2 - (\phi_{sf, strong} - \phi_{sb, strong})}{\phi_t \left(1 - e^{-\left(\frac{\phi_{sf, strong} - \phi_{sb, strong}}{\phi_t} \right)} \right)} + 1 \right) \quad (2.14)$$

where $\phi_{sf, strong}$, $\phi_{sb, strong}$, and $\phi_{sbulk, strong}$ represent the front surface potential, back surface potential, and bulk surface potential in the strong inversion region, respectively. The value of $\phi_{sb, strong}$ is given by (2.9) and $\phi_{sbulk, strong}$ can be acquired from (2.8) and (2.9) as

$$\phi_{sbulk, strong} = \left(-\beta + \sqrt{\beta^2 - \alpha + (\phi_{sf, strong})^2} \right)^2 \quad (2.15)$$

$$\text{where } \beta = 0.5\gamma_{bulk} \left(1 + \frac{C_{box}}{C_{soi}} \right)$$

(2.14) is a nonlinear equation in terms of $\phi_{sf, strong}$ and a direct solution of it cannot be obtained. Two approximations are suggested for (2.14) in the case of bulk and PDSOI MOSFET cases [34], [35]. The first approximation for the surface potential ($\phi_{sf, strong}^1$) used in [35] is given as

$$\phi_{sf, strong}^1 = 2\phi_F + V_{CB} \quad (2.16)$$

However, in [34], it is presented that the use of $\phi_{sf, strong}^1$ results in a large error at the strong inversion region. In [34] it is also presented that a replacement of $\phi_{sf, strong}$ by a value several times higher than $2\phi_F + V_{CB}$ results in a good modeling at strong inversion but erroneous modeling at the moderate inversion region, which is critical for low-voltage designs. Therefore, this approximation was also rejected.

The second approximation $\phi_{sf, strong}^2$ for the surface potential $\phi_{sf, strong}$ recommended by [34] as following:

$$\phi_{sf, strong}^2 = 2\phi_F + V_{CB} + \frac{\phi_{sf, weak} - 2\phi_F - V_{CB}}{\sqrt{1 + \left(\frac{\phi_{sf, weak} - 2\phi_F - V_{CB}}{\eta\phi_t} \right)^2}} \quad (2.17)$$

where, η is a constant and its numerical value is between 4 and 6 to get a improved approximation for ϕ_s in the case of bulk MOSFETs [34], [35]. Hence, η is taken as 6 for the range of doping and oxide thicknesses used in this paper. This approximation results in a

more accurate final solution. Direct use of approximation (2.17) in (2.14) results in discontinuities at two points, which can cause serious problems in circuit simulators, and hence, a sharp increase in simulation time. Therefore, these discontinuities are removed by substituting $2\phi_F + V_{CB}$ in (2.17) by a function f , which is continuous for all values of gate voltage changes from $\phi_{sf,weak}$ at weak inversion to $2\phi_F + V_{CB}$ at strong inversion [6], [34]

$$f = \frac{\phi_{sf,weak} + 2\phi_F + V_{CB} - \sqrt{(\phi_{sf,weak} - 2\phi_F - V_{CB})^2 + 4\delta_2^2}}{2} \quad (2.18)$$

where δ_2 is a fitting parameter and its value is taken as 0.1 [6], [34].

2.4.4 Single piece model

To merge the two solutions of the front surface potential obtained from weak and strong inversion regions, a good smoothing function is needed. The criteria for smoothing function are: 1) it should be continuous and differentiable and 2) it should ensure that each of the approximations for the weak and strong inversions is reduced smoothly to insignificance outside of its respective region of validity. Since the nature of the front surface potentials in the weak and strong inversion conditions is similar to that of a PDSOI MOSFET, a well-known smoothing function is used to satisfy the two aforementioned requirements, which have been successfully used in the case of the PDSOI MOSFET [35]. The smoothing function is given as

$$\phi_{sf} = \phi_{sf,strong} - \phi_t \ln \left(1 + e^{\frac{\phi_{sf,strong} - \phi_{sf,weak}}{\phi_t}} \right) \quad (2.19)$$

(2.19) relies on the statement that in strong inversion, $\phi_{sf,strong} \gg \phi_{sf,weak}$ and in the weak inversion $\phi_{sf,strong} \ll \phi_{sf,weak}$. The continuity and infinite differentiability of the final ϕ_{sf} is confirmed by the continuity and infinite differentiability of all the smoothing functions. After obtaining ϕ_{sf} , the other two surface potentials ϕ_{sb} and ϕ_{sbulk} are obtained by using ϕ_{sf} from (2.19) in (2.8) and (2.9). As there are three variables and values of these variables are obtained from numerical solution of (2.5), (2.8) and (2.9). In order to cross check whether the analytical calculated value from (2.8), (2.9) and (2.19) are matched with the numerical solution (2.5), (2.8) and (2.9) are needed.

2.5 Surface Potential based drain current model

In this section the drain current model based on the surface potential is presented. In order to calculate the drain current Yu et al. model is used. In respect to calculation time consumption it is efficient one. However as mentioned in previous chapter that Yu et al. model has weakness in deriving surface potential so rather than using its surface potential derivation, here, [22] is used for surface potential derivation. The approximations made here

are similar to those made during ϕ_{sf} analytical model derivation; moreover some other approximations are made here. These are (i) the ignoring current component due to the gradient of electron temperature, (ii) the gradual channel approximation and (iii) the charge sheet approximation. The drain current consists of drift and diffusion current components [35], [38]. By assuming that the current is constant along the channel and including series resistance effects [23], short-channel effects [38], self-heating effects [39], the polysilicon depletion effect [40], and the parasitic bipolar effect [41], drain current is given by

$$I_{DS} = \begin{cases} \frac{-b_1 - \sqrt{b_1^2 - 4a_1c_1}}{2a_1} & \text{for } R_D \neq R_S \\ -\frac{c_1}{b_1} & \text{for } R_D = R_S \end{cases} \quad (2.20)$$

where

$$a_1 = WC_{of} \mu_n^0 \eta (R_S + R_D) \frac{R_S - R_D}{2}$$

$$b_1 = -WC_{of} \mu_n^0 (R_S + R_D) \times \left[V_{Gf} - V_{th} + \eta \phi_t - \frac{\eta R_D}{R_S + R_D} (\phi_{sfL} - \phi_{sf0}) \right] - L - \frac{\mu_n^0}{v_{sat}} (\phi_{sfL} - \phi_{sf0})$$

$$c_1 = WC_{of} \mu_n^0 \left[V_{Gf} - V_{th} + \eta \phi_t - \frac{\eta}{2} (\phi_{sfL} - \phi_{sf0}) \right] (\phi_{sfL} - \phi_{sf0})$$

where R_S (R_D) is the source (drain) series resistance, V_{th} is the effective threshold voltage, L is the effective channel length including the channel length modulation, W is the channel width, η is a factor describing the bulk charge effects, μ_n^0 is the mobility at a given gate voltage and bulk voltage, μ_0 is the maximum low field mobility in the inversion layer, here we assume $\mu_0 = \mu_n^0$, v_{sat} is carrier saturation velocity [23], [38] and [39]. The drain current I_{DS} in (2.20) is expressed as a function of the surface potential at the source side ϕ_{sf0} and at the drain side ϕ_{sfL} . The front surface potential ϕ_{sf} is obtained from the analytical surface potential model in section 2.4.

Chapter 3

Quantum Mechanical Effect

Quantum mechanical (QM) effects are playing a significant role in SOI MOSFETs surface potential characteristics due to the ever shrinking feature size. Usually quantum mechanical effects are taking place for SOI MOSFETs in deep sub-micron region which means their channel length is in nanometer scale. Energy quantization in silicon film is a major quantum mechanical effect occurring in a SOI MOSFET at deep sub-micron region. So in this case, semi-classical models are inadequate to model the device precisely, which will lead to erroneous and misleading predictions of critical device structure and electrical behavior parameters such as the physical oxide thickness, threshold voltage, drive current, surface potential, gate capacitance and sub-threshold swing.

3.1 Energy quantization in the Silicon film due to quantum mechanical effects

As the dimensions of the devices approach deep submicron and nanometer regions, the classical movement of the charge carriers is greatly affected by the non-classical behavior of electrons in the SOI MOSFETs. The scaling down of SOI MOSFETs is accomplished by the result of thinner oxide and smaller device size which leads to the improvement of electric field at different interfaces. For very high electric fields in the silicon/silicon oxide interfaces, the potential at the interfaces becomes steep. So a potential well is formed by the oxide barrier and the silicon conduction band under inversion condition. The carriers are confined in this narrow potential well. Because of the confinement of the carriers, inversion layer electrons must be treated quantum mechanically as a two dimensional electron gas. Due to this confinement, the electron energies are quantized and hence the electrons occupy only discrete energy levels. This results in the electrons residing in some discrete energy levels as shown in Figure 3.1 which are above the classical energy level.

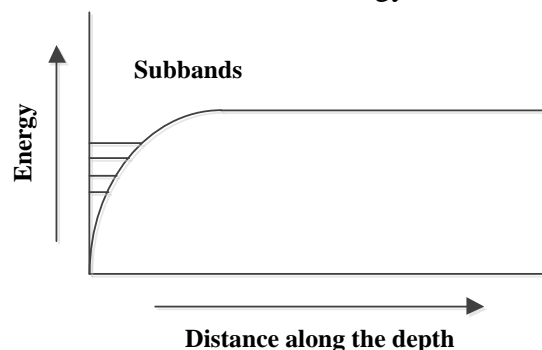


Figure 3.1: Discrete energy levels due to quantization (in the substrate).

Due to the narrow potential well the motion of the carriers of the surface channel is quantized in the direction perpendicular to the interface; consequently the carrier (probability) density is at maximum inside the well and not at the boundaries, as shown in Figure 3.2. In addition, the minimum energy for the electrons in the conduction energy

subbands increases with the electron concentration. This effect reduces the current drive of the device and is not predicted by classical simulators [42]. Therefore, the operation of deeply scaled SOI transistors cannot be accurately described by semi-classical physics, and accurate calculation of the inversion charge requires introducing concepts derived from quantum mechanics (QM).

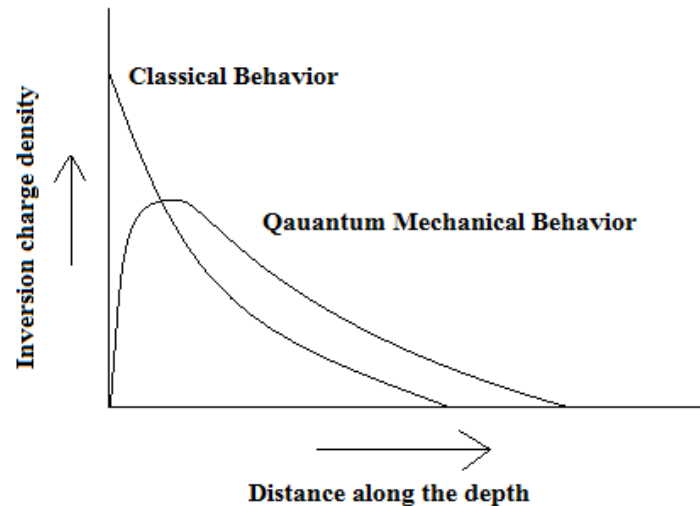


Figure 3.2: Electron concentration distribution in the silicon substrate in classical and quantum mechanical cases.

3.1.1 Threshold Voltage shift

It is found that, due to quantum confinement of carriers in a thin silicon layer, the minimum energy for electrons in the conduction band increases when the thickness of the silicon film is reduced. As a result, the threshold voltage increases as the film thickness is reduced. Furthermore, the minimum energy for the electrons in the conduction energy sub bands increases with the electron concentration, which dynamically increases the threshold voltage [42]. The carrier confinement in very narrow potential well is governed by the wave functions and energy levels of the various sub bands. As the film becomes thinner than 10 nm, the energy levels and their separation increases, making them harder to populate, so the threshold voltage increases.

3.1.2 Shift in surface potential

According to the semi-classical model at strong inversion surface band bending will be almost fixed. At this situation slight increase in surface potential results in a large build up of electron density at the surface. Devices with gate oxide in nanometer range results in high electric field so the surface band bending from the quantum mechanical model is considerably larger than that from the classical model. This is because the 2-D carrier distribution of the sub bands and discrete energy levels lead to reduced charge density

compared to semi-classical calculation. As a result an additional band bending is required for an increased charge density. So this results to increase in surface potential. Therefore, the operation of deeply scaled SOI transistors cannot be accurately described by semi-classical physics, accurate calculation of the inversion charge requires introducing concepts derived from quantum mechanics (QM).

3.2 Quantum Mechanical Correction to the Surface Potential of Nanoscale FD SOI MOSFETs

Different techniques and models have been proposed over the years to incorporate the quantum mechanical effects for MOS transistors, which can be used for SOI transistors as well. Such as band-gap widening model which indirectly includes quantum mechanical (QM) correction [31]. In this model, the proposed QM correction requires transformation of the semi-classical model. The existing physically based QM corrections are either derived from triangular well approximation or variational technique [2]. The physics of both approaches are dependable but none of the techniques are quantitatively correct. A physically based explicit analytical model for the QM correction the surface potential of nanoscale MOS devices was proposed in [32]. Recent study showed this model provides a more accurate QM correction method than the previous ones over a large range of device parameters.

3.2.1 Basic approach of the Karim and Haque QM model

The Karim and Haque QM correction model to the semi-classical surface potential (ϕ_{sf}), is valid for both MOS and SOI devices. This model directly adds the QM correction term to the semi-classical ϕ_{sf} , instead of applying indirect band-gap widening approach.

As the Karim and Haque QM model dictated according to the semi-classical charge sheet model, the inversion carriers are treated as a sheet charge at the Si-film–front-oxide interface of SOI MOSFET. Under the inversion bias due to the QM effect quantization of the energies of the mobile charge carriers occurred which is discussed in section 3.1. According to the QM charge sheet model, the effect of QM shifts the sheet charge corresponding to the quantized charge carriers into front Si of UTB SOI MOSFET by an amount. The amount of shift is called Z_{av} here, which is the average distance of charges from the Si-film–front-oxide interface considering the QM effect. This is the primary reason of increase in front surface potential (ϕ_{sf}) due to QM effect. Most existing surface-potential-based models use the band-gap widening approach to incorporate QM correction to the semi-classical ϕ_{sf} . On the other hand in this model they are using the physics of the QM charge sheet model and propose the correction to the surface potential due to the QM effect as

$$\delta\phi_{sf} = -\frac{Q_{inv}Z_{av}}{\epsilon_0\epsilon_{Si}} \quad (3.1)$$

where Q_{inv} is the inversion layer charge density.

The surface potential $\phi_{\text{sf[qm]}}$ including the QM effect is expressed as

$$\phi_{\text{sf[qm]}} = \phi_{\text{sf[sc]}} + \delta\phi_{\text{sf}} \quad (3.2)$$

Here, $\phi_{\text{sf[sc]}}$ is the semi-classical front surface potential neglecting QM effects, which can be estimated from the equations of [44] by considering the effect of substrate charge explicitly. For calculating the $\phi_{\text{sf[qm]}}$ we only consider front surface potential and neglect other surface potential of SOI MOSFET. We only investigate the QM effect on the drain current of the UTB SOI MOSFET. In order to obtain the drain current from surface potential we use (2.20) where only front surface potential is needed. So, we neglect other surface potential of UTB SOI MOSFET for incorporating the QM effect on surface potential and drain current.

The energies of the quantized states are proportional to $F_{\text{ox}}^{2/3}$ according to the Airy function approximation, where F_{ox} is the oxide electric field. For the state-of-the-art nanoscale MOSFETs, the two-third power law which is stated above is not accurate. Though, this approximation provides a simple analytical expression for QM correction. However, it has been shown that the quantized energies of the quasi-bound states follow a power-law relationship, as functions of F_{ox} , which is different from the two-third power law, as predicted by the Airy function approximation, even when the wave function penetration effect into the gate dielectric is considered. The energy of the lowest quasi-bound state E_1 is measured from the respective band edge. E_1 Expressed in [46] is as:

$$E_1 = \zeta_1 \left(\frac{|F_{\text{ox}}| \text{cm}}{\text{MV}} \right)^\lambda \quad (3.3)$$

Here, $\zeta_1 = 77\text{meV}$ and $\lambda = 0.61$ for electrons, and $\zeta_1 = 88\text{meV}$ and $\lambda = 0.64$ for holes incorporating the wave function penetration effect. The penetration of the wave function into the oxide increases with shrinking gate oxide thickness and increasing substrate doping concentration [47]. Precise evaluation of the quantized eigen energy levels in the semiconductor region depends on the amount of this wave function penetration into the oxide region. The wave function has to be taken into account. Z_{av} is reduced when wave function penetration effect is taken into account for a given semiconductor charge density. As a result of reduction in Z_{av} magnitude of the surface potential is also being reduced.

Z_{av} Can be written as:

$$Z_{\text{av}} = \frac{E_1}{qF_s} \quad (3.4)$$

where F_s is the electric field at the gate oxide, Si film interface of UTB SOI.

3.2.2 Derivation of a mathematical expression of the proposed QM model

In the inversion region inversion charge density $Q_{\text{inv}} = Q_s - Q_b$ which can be expressed as:

$$Q_{\text{inv}} = -C_{\text{ox}}(V_g - V_{\text{FB}} - \phi_{\text{sf}[\text{qm}]}) - Q_b \quad (3.5)$$

where $C_{\text{ox}} = (\epsilon_0 \epsilon_{\text{ox}} / T_{\text{ox}})$ is the oxide capacitance per unit area, V_{FB} is the flat-band voltage,

$Q_b = \mp \gamma C_{\text{ox}} \sqrt{|\phi_{\text{sf}[\text{qm}]}|}$ is the depletion charge density, and $\gamma = \frac{\sqrt{2qN_{\text{ch}}\epsilon_0\epsilon_{\text{si}}}}{C_{\text{ox}}}$ is the body

factor. Here, the (-) sign is for n-MOS devices, and the (+) sign for p-MOS devices. An implicit equation for $\delta\phi_{\text{sf}}$ can be obtained by substituting (3.5) into (3.1) and using (3.2). This implicit equation can be solved iteratively. For computational efficiency the numerical solution of the implicit equation is not smart.

It has numerically been verified that $\delta\phi_{\text{sf}}$ shows satisfactory convergence after the first two iterations. An explicit analytical expression for $\delta\phi_{\text{sf}}$ can be derived considering only the first two iterations, which are expressed as:

$$\delta\phi_{\text{sf}} = \frac{C_{\text{ox}} \left[V_g - V_{\text{fb}} - \left(\phi_{\text{sf}[\text{sc}]} + \delta\phi_{\text{sf}}^1 \pm \gamma \sqrt{|\phi_{\text{sf}[\text{sc}]} + \delta\phi_{\text{sf}}^1|} \right) \right] E_1^1}{q\epsilon_0\epsilon_{\text{ox}} F_{\text{ox}}^1} \quad (3.6)$$

And $\delta\phi_{\text{sf}}^1$, the first order solution is

$$\delta\phi_{\text{sf}}^1 = \frac{C_{\text{ox}} \left[V_g - V_{\text{fb}} - \left(\phi_{\text{sf}[\text{sc}]} \pm \gamma \sqrt{|\phi_{\text{sf}[\text{sc}]|} \right) \right] E_1^0}{q\epsilon_0\epsilon_{\text{ox}} F_{\text{ox}}^0} \quad (3.7)$$

Here, the (+) signs are for n-MOS devices, and the (-) signs are for p-MOS devices. E_1^0 and F_{ox}^0 are the zeroth-order terms, and E_1^1 and F_{ox}^1 are the first-order terms respectively. These are given by:

$$E_1^0 = \zeta_1 \left(\frac{|F_{\text{ox}}^0| \text{cm}}{\text{MV}} \right)^\lambda \quad (3.8)$$

$$E_1^1 = \zeta_1 \left(\frac{|F_{\text{ox}}^1| \text{cm}}{\text{MV}} \right)^\lambda \quad (3.9)$$

$$F_{\text{ox}}^0 = \frac{C_{\text{ox}} (V_g - V_{\text{fb}} - \phi_{\text{sf}[\text{sc}]})}{\epsilon_0\epsilon_{\text{ox}}} \quad (3.10)$$

$$F_{\text{ox}}^1 = \frac{C_{\text{ox}} [V_g - V_{\text{fb}} - (\phi_{\text{sf}[\text{sc}]} + \delta\phi_{\text{sf}}^1)]}{\epsilon_0\epsilon_{\text{ox}}} \quad (3.11)$$

The main result which can be added to the semi-classical surface potential to attain QM corrected result is $\delta\phi_{sf}$ here.

From (3.6) and (3.7) it can be realized that surface potential with QM effect leads to diverging derivative with respect to the gate voltage at flat-band V_{FB} . It has been founded by using numerical verification that $\delta\phi_{sf}$ is negligible around the flat-band [32]. The problem of diverging derivative has been overcome exploiting this observation. It has done as follows:

$$\begin{aligned}\phi_{sf[qm]} &= \phi_{sf[sc]}, V_{tr1} \leq V_{gs} - V_{FB} \leq V_{tr2} \\ &= \phi_{sf[sc]} + \delta\phi_{sf} \quad \text{otherwise}\end{aligned}\tag{3.12}$$

Here, V_{tr1} and V_{tr2} are two transition voltages such that $V_{tr1} < 0$ and $V_{tr2} > 0$. Choices for $V_{tr1} = -0.001$ V and $V_{tr2} = 0.2$ V for n-MOS and for p-MOS devices, $V_{tr1} = -0.15$ V and $V_{tr2} = 0.001$ V that work well for all cases.

Chapter 4

Results and Discussion

In our work we have analyzed the surface potentials for all the three surfaces (gate oxide–silicon film interface, silicon-film–buried oxide interface, and buried oxide–substrate interface) of fully depleted silicon-on-insulator (SOI) MOSFETs by considering the effect of substrate charge explicitly and hence obtain I-V characteristics based on the surface potential based compact model. As already mentioned in the previous discussions due to ultra thin body of the UTB SOI MOSFET the semi-classical models become inadequate. So, the Quantum mechanical effects need to be considered. So, finally we include quantum mechanical effect in surface potential to analyze the impact of quantum mechanical correction to the surface potential based compact model on the drain current of UTB SOI MOSFET.

4.1 Surface Potential

For calculating surface potential we choose [22] where it is assumed that no inversion takes place at the back surface and the silicon layer is fully depleted. Most of the parameter values are also taken from [22]. Values of all the parameters used in our model are given in the following table.

Table 4.1: Parameter used in surface potential model verification

Parameter	Value
Dielectric constant of Silicon	11.7
Dielectric constant of Silicon-di-oxide	3.9
Front oxide thickness, t_{ox}	3 nm
Silicon film thickness, t_{soi}	8 nm, 25 nm
Buried oxide thickness, t_{box}	16 nm, 50 nm
Silicon Film doping, N_{ch}	10^{17} cm^{-3}
Substrate doping, N_{sub}	10^{15} cm^{-3}
Silicon Intrinsic carrier concentration, n_i	$1 \times 10^{10} \text{ cm}^{-3}$
Room Temperature	300 K
Flat band voltage, V_{FB}	0.5 V
Substrate voltage, V_{sub}	0 V

For calculating surface potentials for all three surfaces first we calculate ϕ_{sf} . In order to do so first we solve (2.5), (2.8), and (2.9) iteratively and plot the exact solution of ϕ_{sf} then the analytical strong inversion surface potential solution obtained from (2.14), (2.16), and (2.17). By using (2.16) and (2.17) in the right side of (2.14) we obtain Approximations 1 and

2 respectively which are basically two solution of $\phi_{sf, strong}$ then we compare it with the iterative solution of ϕ_{sf} .

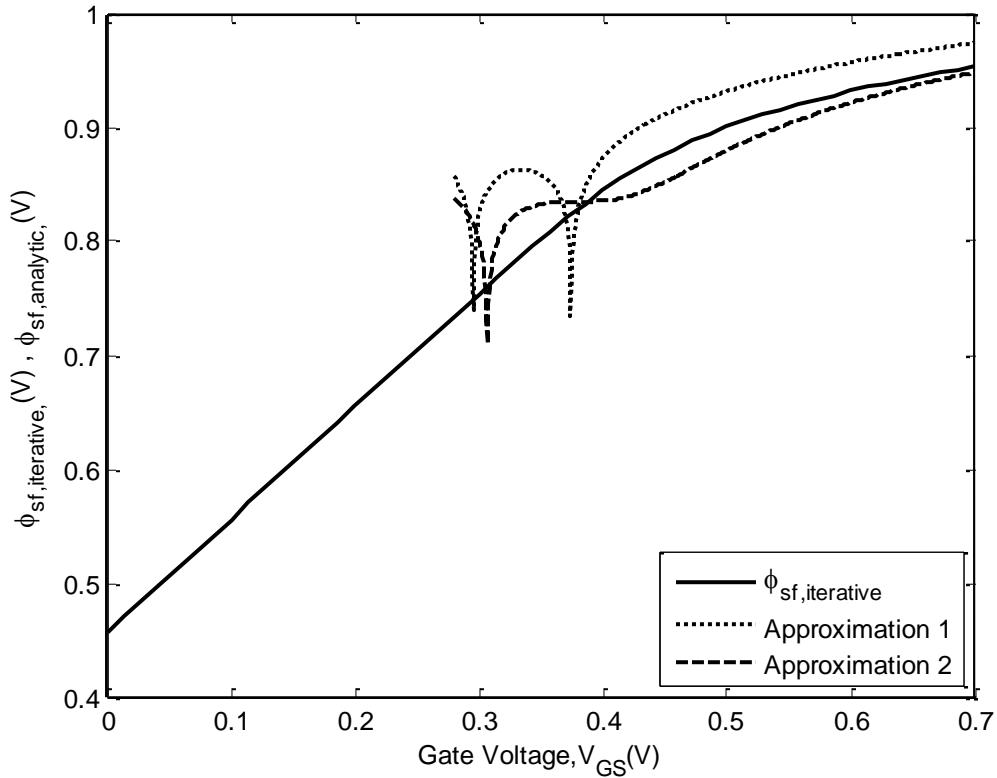


Figure 4.1: For FD SOI, comparison of ϕ_{sf} obtained iteratively and analytically. Here, $t_{soi} = 25$ nm and $t_{box} = 50$ nm.

Figure 4.1 shows a comparison between the exact solution of the front surface potential which we get from iteration and the analytical strong inversion surface potential solution. From above figure we observe that Approximation 2 is closer to the exact solution.

In Figure 4.2 elimination of the discontinuities is presented. The figure displays the plots of $\phi_{sf, weak}$, $\phi_{sf, strong}$, obtained from (2.14) and (2.16)–(2.18), and the iterative solution of the surface potential, acquired from (2.5), (2.8), (2.9). In both the weak and strong inversion regions good match is achieved. Moreover, in the strong inversion solution, no discontinuity is observed.

In order to obtain analytical surface potentials ϕ_{sf} , ϕ_{sb} , and ϕ_{sbulk} we used (2.19), (2.14), and (2.15). Afterward we compare them with numerically solved surface potentials which are obtained by using (2.6), (2.14), and (2.15).

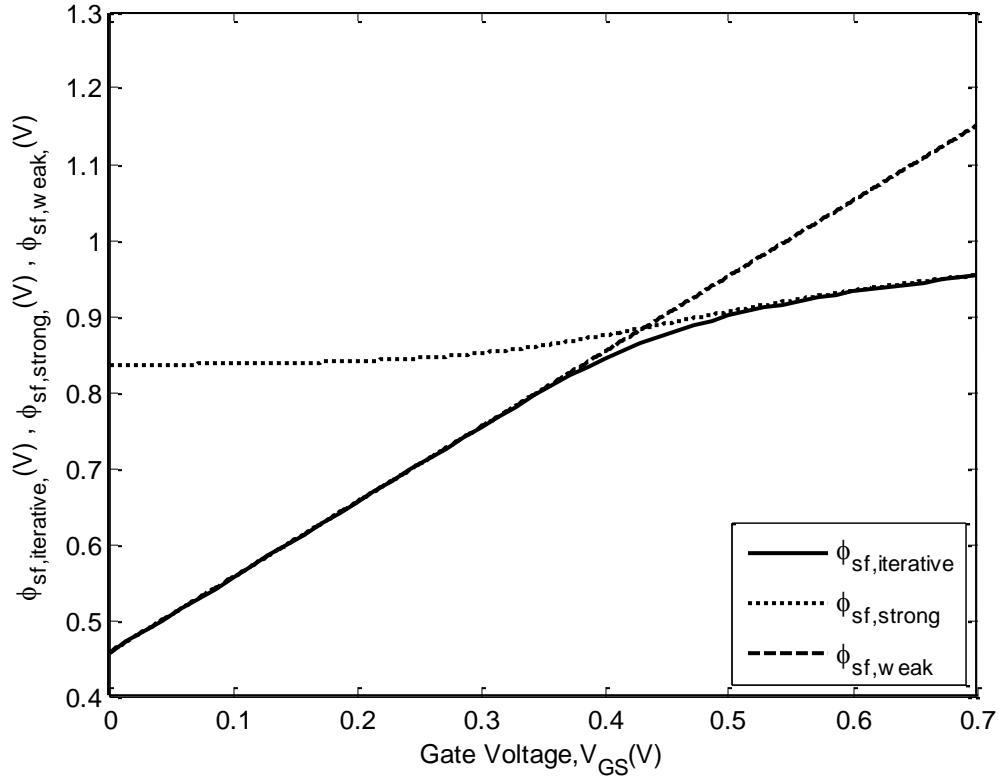


Figure 4.2: For FD SOI, $\phi_{sf,weak}$, $\phi_{sf,strong}$, and $\phi_{sf,iterative}$ versus gate voltage. Here, $t_{soi} = 25$ nm and $t_{box} = 50$ nm.

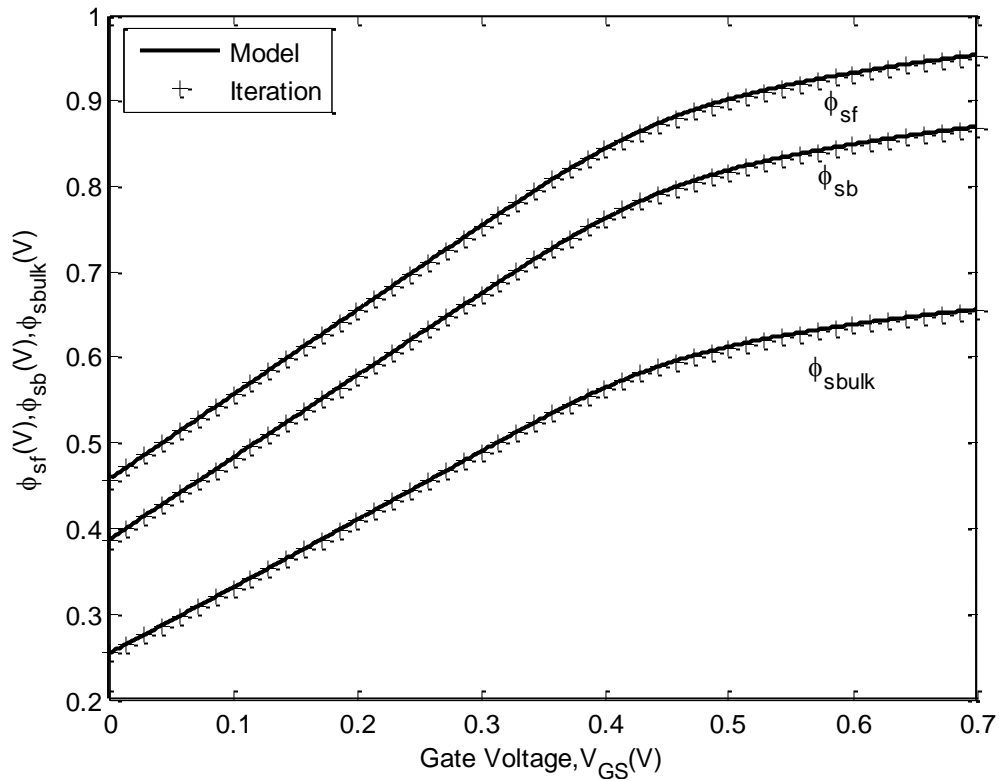


Figure 4.3: For FD SOI, three surface potentials ϕ_{sf} , ϕ_{sb} , and ϕ_{sbulk} versus gate voltage. Here, $t_{soi} = 25$ nm and $t_{box} = 50$ nm.

The variation of surface potentials ϕ_{sf} , ϕ_{sb} , and ϕ_{sbulk} versus the gate voltage is observed in Figure 4.3. To clearly demonstrate the effect of substrate depletion charge on the front surface potential the substrate doping is selected quite low (10^{15} cm^{-3}). A large potential drop appears across the substrate depletion region, when the substrate doping is low, which changes the channel inversion charge density significantly. Figure 4.3 undoubtedly demonstrates a large drop across the substrate region given by ϕ_{sbulk} . The surface potentials from the analytical solution are in close proximity with the iterative results.

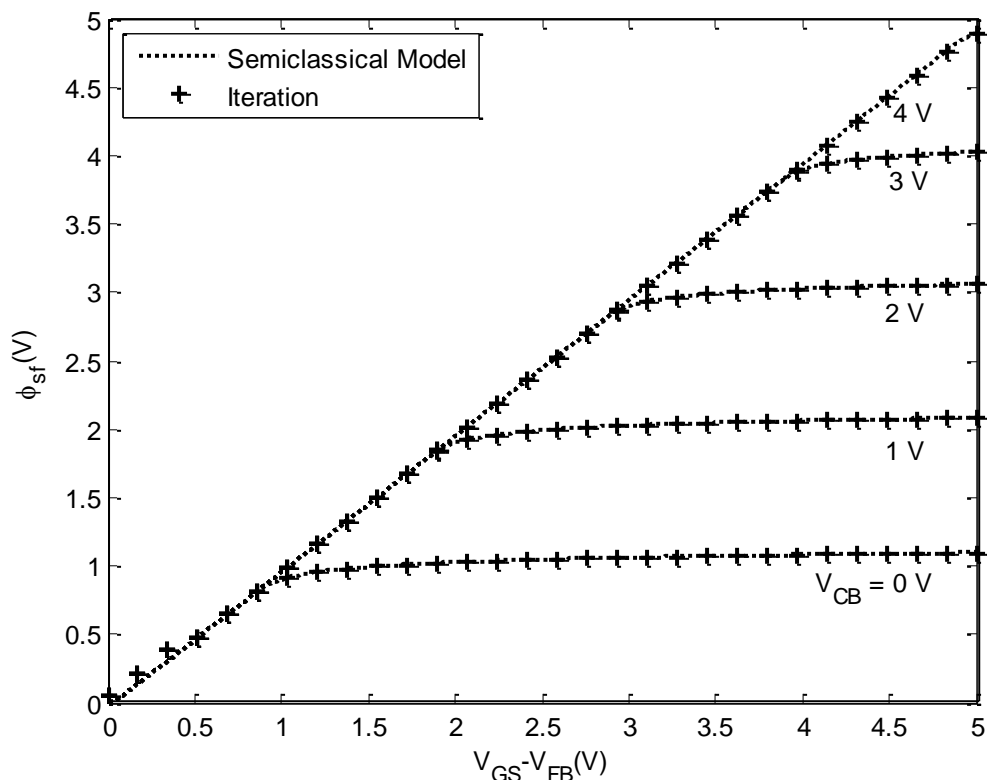


Figure 4.4: For FD SOI, ϕ_{sf} versus gate voltage for different values of V_{CB} . Here, $t_{soi} = 25 \text{ nm}$ and $t_{box} = 50 \text{ nm}$.

In order to obtain semi-classical front surface potential ϕ_{sf} analytically for FD SOI MOSFET we use (2.19) and then we compare ϕ_{sf} with numerically solved surface potentials which are obtained by solving (2.6), (2.14), and (2.15) iteratively. The result is shown in Figure 4.4.

To obtain quantum correction of ϕ_{sf} of UTB SOI we use (3.12). For obtaining $\phi_{sf[sc]}$ we used the same approach as used for obtaining ϕ_{sf} of FD SOI MOSFET. However for UTB SOI we take $t_{soi} = 8 \text{ nm}$. In this case we found a maximum relative error of 0.6% between the analytical solution of three surface potentials and iterative solution of exact Poisson equation. The relative error is calculated using the following formula

$$\text{Relative error} = \frac{\text{Analytical solution} - \text{Iterative solution}}{\text{Iterative solution}} \times 100\%$$

Figure 4.5 shows variation of ϕ_{sf} with gate voltage for different values of the channel floating voltage V_{CB} . We notice that the surface potential varies linearly in the weak inversion region and then saturates at high values of gate voltages similar to that observed in the case of bulk MOSFETs. The simulation results are in close proximity with the results obtained from the iterative solution of the Poisson equation.

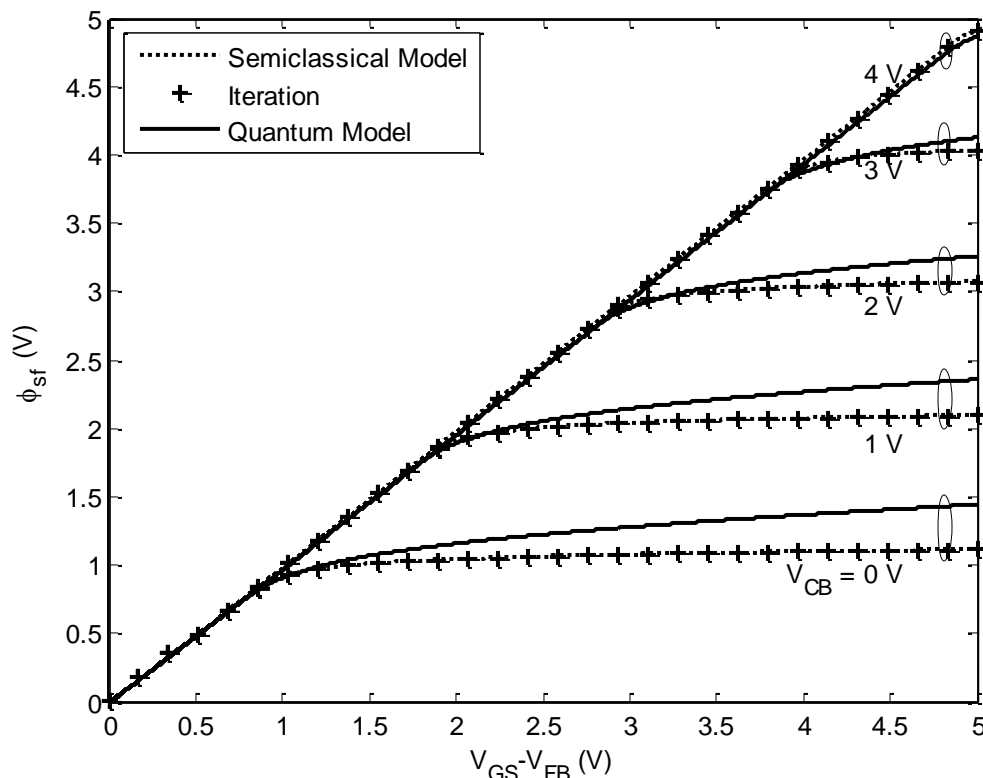


Figure 4.5: For UTB SOI, ϕ_{sf} versus gate voltage for different values of V_{CB} with QM correction. Here, $t_{soi} = 8$ nm and $t_{box} = 50$ nm.

As we discussed in the section 3.1.2, including quantum mechanical effect in surface potential increases surface potential. The result is shown in the Figure 4.5. From Figure 4.5 it is also observed that for higher value of V_{CB} we get almost same front surface potential from semi-classical and quantum mechanical model in this figure. The reason of this is as we increase V_{CB} , weak inversion is extended and it still doesn't reach the strong inversion. As discussed in the section 3.1.2 lack of charge carrier density in the Silicon film is the reason of increase in front surface potential, so here ϕ_{sf} is not increased so much.

4.2 Drain Current

For FD SOI MOSFET we calculate drain current using (2.20) which need front surface potential ϕ_{sf} for its calculation. The result is given in Figure 4.6.

In case of UTB SOI MOSFET we calculate the drain current for both semi-classical and quantum mechanical model using (2.20) which require front surface potential ϕ_{sf} for its calculation.

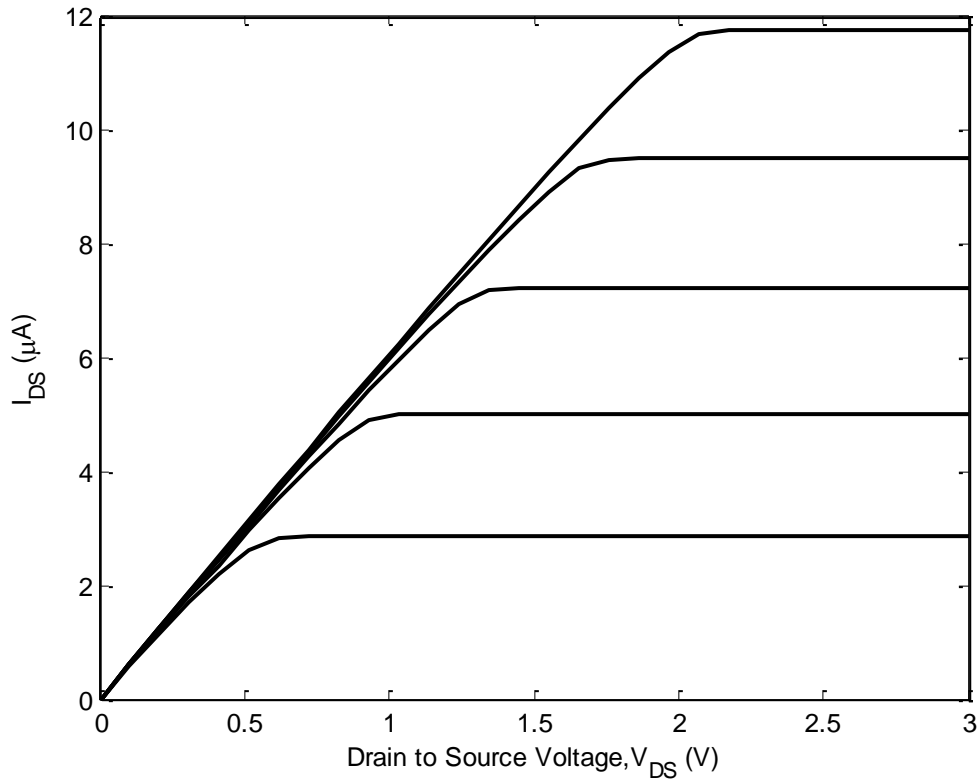


Figure 4.6: For FD SOI, V_{DS} versus I_{DS} for different V_{GS} . Here, $t_{soi} = 25$ nm and $t_{box} = 50$ nm.

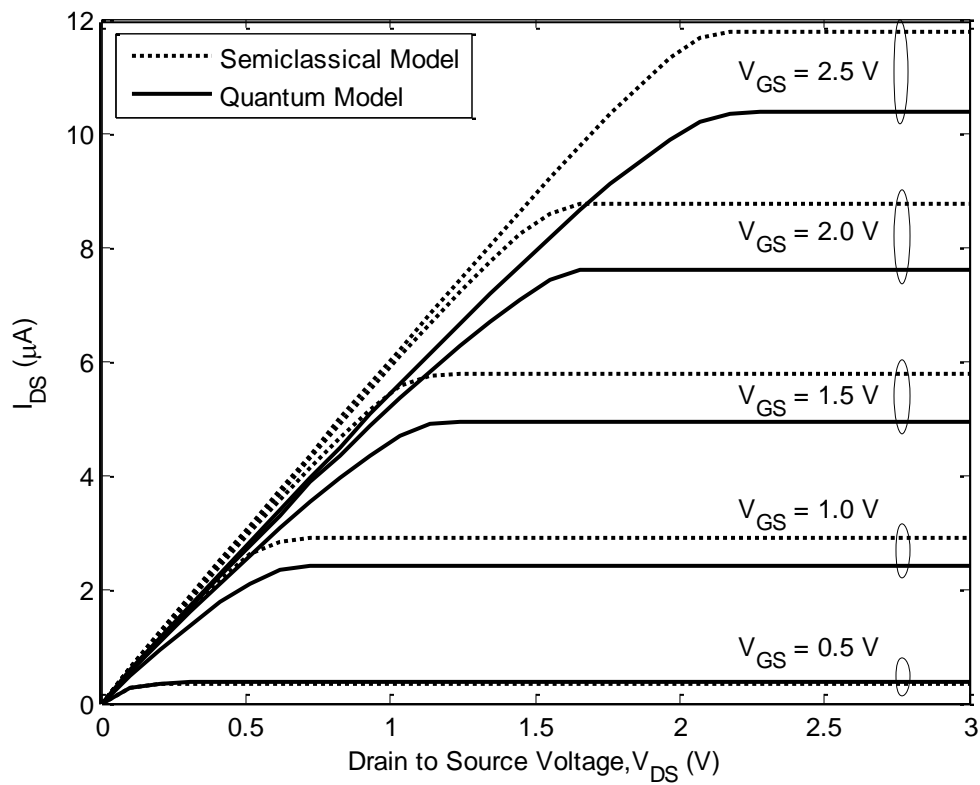


Figure 4.7: For UTB SOI, V_{DS} versus I_{DS} for different V_{GS} including QM correction of Drain current. Here, $t_{soi} = 8$ nm and $t_{box} = 50$ nm.

For semi-classical model ϕ_{sf} is obtained from (2.19) and for quantum mechanical model ϕ_{sf} is obtained from (3.12). Result is given in Figure 4.7.

Table 4.2: Percentage difference of Saturation Current

V_{GS} (V)	$I_{DS(sat)}$ (SC) μA	$I_{DS(sat)}$ (QM) μA	Percentage difference
2.5	11.78	10.36	12.05
2	8.76	7.61	13.13
1.5	5.78	4.93	14.71
1	2.88	2.41	16.32
0.5	0.35	0.36	2.86

Table 4.3: Difference of V_{DS} for obtaining transition point

V_{GS} (V)	$V_{DS(tran)}$ (SC) V	$V_{DS(tran)}$ (QM) V	Difference (V)
2.5	2.27	2.27	0.00
2	1.79	1.77	0.02
1.5	1.31	1.31	0.00
1	0.81	0.82	0.01
0.5	0.39	0.38	0.01

In Figure 4.7 we observe semi-classical analytical compact model, and quantum corrected model of drain current vs. V_{DS} for various V_{GS} . As we used Karim and Haque model [32] for quantum mechanical correction and in Karim and Haque model it is mentioned that it include quantum mechanical effect by considering wave function penetration through the gate oxide, so here we see that drain current obtained from quantum model is less than the drain current obtained from semi-classical model. At the same gate voltage (V_{GS}) inversion carrier density is lower for the QM effect, as a result QM corrected drain current is lower than semi-classical model.

From Table 4.2 it is found that, with the change of V_{GS} percentage difference between semi-classical and QM corrected drain current is almost constant, but at $V_{GS} = 0.5V$ this assumption is not correct because here threshold voltage, $V_{th} = 0.346V$, so device does not reach strong inversion at this point and two current is almost the same. In Table 4.3 we observe slight change in transition voltage between quantum model and Semi-classical model for different value of V_{GS} . For a fixed V_{GS} transition voltage is the voltage between the linear region and the saturation region of the I_{DS} - V_{DS} characteristics.

Chapter 5

Summary

5.1 Conclusion

In our work we have studied the impact of Quantum Mechanical correction on the drain current of UTB SOI MOSFET. We included the quantum mechanical effect into front surface potential of UTB SOI MOSFET by using Karim and Haque model [32]. Surface potential based compact model of FD SOI MOSFET is used to obtain semi-classical ϕ_{sf} for UTB SOI MOSFET.

Prior to studying the impact of Quantum Mechanical Effect on surface potential we have studied a closed-form surface potential solution for all the three surfaces of the FD SOI MOSFET. The effect of substrate charge is considered explicitly. We observed that if the doping density of the substrate is varied then back surface potential for SOI structure also varied. Closed form of surface potential solution is derived from the solution of 1-D Poisson equation.

We observed that the insertion of QM correction into the front surface potential (ϕ_{sf}) of UTB SOI MOSFET increases ϕ_{sf} . QM correction results decrease of drain current in strong inversion region of the UTB SOI MOSFET. In comparison with semi-classical model the increase of ϕ_{sf} and decrease of drain current is observed.

In section 3.1.2, it is discussed that including quantum mechanical effect in surface potential will increase surface potential. The lack of charge carrier density in the Silicon film is the reason of increase in front surface potential. The drain current obtained from quantum model is less than the drain current obtained from semi-classical model.

5.2 Future Work

Further extension of our work can be done more accurately and comprehensively. As the channel length L is reduced to increase both the operation speed and the number of components per chip, short-channel effects arise such as drain-induced barrier lowering, velocity saturation, and impact ionization. These short channel effects can be included to make this model more realistic. Our work is based on 3 nm gate oxide. And for thinner gate oxides, gate leakage current is significant which can be analyzed. Here we use constant mobility, but mobility depends on several factors which can be included in future work. Moreover, removal of excess heat generated within the SOI devices is less efficient than in bulk devices, which may result in a substantial increase in device operating temperature and the phenomenon is called self heating effect. Self heating is due to the thermal isolation of transistors from the substrate by the buried insulator. In future one can incorporate the thermal variation of the device. One can also analyze the effect of parasitic capacitance over this model. Besides, comparison between other models can be made to have a better idea of the device performance. With the decreasing length of the channel, ballistic Quantum

transport is playing a vital role. So, further improvement of this model should do by incorporating the ballistic transport effect.

Appendix

Matlab code for obtaining figure 2.3, figure 2.5 and figures in Result section :

```
% Matlab 10 (version 10) is used in writing and simulation of the code
function utbsoi

clc
clear all

q=1.602e-19; % Charge magnitude of electron (C)
eta=6; % A factor describing the bulk charge effects
delta2=0.1; % A fitting parameter

% All units are converted into cm,cm^2,cm^3.

esi=11.7*8.854e-14; % Dielectric constant of Silicon [F/cm]
eox=3.9*8.854e-14; % Dielectric constant of Silicon Dioxide [F/cm]

tox=3e-7; % Front oxide thickness [cm]
tsoi=8e-7; % Silicon film thickness [cm]
tbox=50e-7; % Buried oxide thickness [cm]

Cox=eox/tox; % Front oxide capacitance per unit area [F/cm^2]
Csoi=esi/tsoi; % Silicon film capacitance per unit area [F/cm^2]
Cbox=eox/tbox; % Buried oxide capacitance per unit area [F/cm^2]
Ceff=1/((1/Cox)+(1/Cbox)+(1/Csoi));
% Series capacitance per unit area [F/cm^2]

Nch=1e17; % Silicon film doping(in which channel formed) [cm^-3]
Nsub=1e15; % Substrated doping(or impurity in bottom silicon part) [cm^-3]

W=10e-4; % Silicon film width [cm]
L=0.1e-4; % Silicon film length [cm]

mu_n=1350; % mobility of electron for Silicon,Si at temperature=300K
Rs=(80000e-3)/W; % source series resistance
v_sat=1e7; % Carrier saturation velocity

phi_t=0.0259; % Thermal voltage at 300k [V]
ni=1e10; % Silicon intrinsic carrier concentration per unit area [cm^-3]
phi_f=phi_t*log(Nch/ni); % Fermi potential [V]

VFB=-0.5; % Flat band voltage mentioned [V]
Vgs=linspace(0,0.7,1000); % This Vgs for analytical model plot. One should
%take a lot of point otherwise for fig(1) shape does not appear correctly.
Vg=Vgs-VFB; % For analytical model
Vcb=0; % Channel floating voltage
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%phi_sf_strong_calc where Vcb=0,Nsub=1e15
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Vgsi=linspace(0,0.7,50); % This Vgsi for iteration plot. Here few points
%are taken for faster computation. If one wants to find the relative error
%then Vgsi must be equal to Vgs.
Vgi=Vgsi-VFB; % This Vgi for iteration
[phi_sf_iter,phi_sb_iter,phi_sbulk_iter]=phi_calc_iter(Vgi,Vcb);% function
% derived in the function derivation section

[phi_sf_strong,phi_sb_strong,phi_sbulk_strong,phi_sf_strong1,...
 phi_sb_strong1,phi_sbulk_strong1,phi_sf_strong2,phi_sb_strong2,...
 phi_sbulk_strong2]=phi_strong_calc(Vg,Vcb);% function derived in the
%function derivation section

figure(1)
plot(Vgsi,abs(phi_sf_iter),'k','LineWidth',2)
hold on
plot(Vgs(Vgs>0.28),abs(phi_sf_strong1(Vgs>0.28)),':k','LineWidth',2)
```

```

hold on
plot(Vgs(Vgs>0.28),abs(phi_sf_strong2(Vgs>0.28)),'--k','LineWidth',2)
hold on
xlabel('Gate Voltage,V_G_S (V)')
ylabel('\phi_s_f,i_t_e_r_a_t_i_v_e,(V) , \phi_s_f,a_n_a_l_y_t_i_c,(V)')
legend('\phi_s_f,i_t_e_r_a_t_i_v_e','Approximation 1','Approximation 2',4)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% phi_sf_weak and phi_sf_strong calculation and comparing them with phi_sf
% iteration here Nsub=1e15 & Vcb not used
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

[phi_sf_weak]=phi_weak_calc(Vg);
% function derived in the function derivation section

figure(2)
plot(Vgsi,abs(phi_sf_iter),'k','LineWidth',2)
hold on
plot(Vgs,abs(phi_sf_strong),':k','LineWidth',2)
hold on
plot(Vgs,abs(phi_sf_weak),'--k','LineWidth',2)

xlabel('Gate Voltage,V_G_S (V)')
ylabel('\phi_s_f,i_t_e_r_a_t_i_v_e,(V) , \phi_s_f,s_t_r_o_n_g,(V) , \phi_s_f,w_e_a_k,(V)')
legend('\phi_s_f,i_t_e_r_a_t_i_v_e' , '\phi_s_f,s_t_r_o_n_g' , '\phi_s_f,w_e_a_k',4)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Three surface potentials analytical model and numerical model comparison
% section phi_sf_calc where Vcb=0,Nsub=1e15
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

[phi_sf,phi_sb,phi_sbulk]=phi_calc(); % function derived in the function derivation section

figure(3)
plot(Vgs,phi_sf,'k','LineWidth',2)
hold on
plot(Vgsi,abs(phi_sf_iter),'+k',Vgsi,abs(phi_sb_iter),'+k',Vgsi,abs(phi_sbulk_iter),...
'+k','LineWidth',1)% mentioned here to get the legend correctly
% otherwise it can be mentioned below
hold on
plot(Vgs,phi_sb,'k','LineWidth',2)
hold on
plot(Vgs,phi_sbulk,'k','LineWidth',2)

xlabel('Gate Voltage,V_G_S (V)')
ylabel('\phi_s_f (V),\phi_s_b (V),\phi_s_b_u_l_k (V)')
legend('Model','Iteration',2)%2 means top left corner, 4 means top right corner
text(0.57,0.68,'\phi_s_b_u_l_k')
text(0.57,0.9,'\phi_s_b')
text(0.57,0.98,'\phi_s_f')
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% %Relative error calculation section between analytical and numerical model
% %To calculate relative error Vgs and Vgsi must be same size
% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% % x=((phi_sf-phi_sf_iter)./phi_sf_iter)*100;
% % y=(phi_sb-phi_sb_iter)./phi_sb_iter)*100;
% % z=(phi_sbulk-phi_sbulk_iter)./phi_sbulk_iter)*100;
% figure(4)
% plot(Vgs,abs(x))
% hold on
% plot(Vgs,abs(y))
% hold on
% plot(Vgs,abs(z))
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Effect of substrate charge on the Surface Potential phi_sbulk_calc for
% different Nsub, where Vcb=0
% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

```

nsub=[1e15,5e15,1e16,5e16]; % Substrated doping(or impurity in bottom silicon part) [cm^-3]
for i=1:length(nsub)
    Nsub=nsub(i);
    % Following two functions are derived in the function derivation
    % section
    [~,~,phi_sbulk_iter]=phi_calc_iter(Vgi,Vcb); % ~ sign used to neglect that specific
    % parameter
    [~,~,phi_sbulk]=phi_calc(); % ~ sign used to neglect that specific parameter
    figure(5)
    plot(Vgs,phi_sbulk,'k','LineWidth',2)
    hold on
    plot(Vgsi,phi_sbulk_iter,'+k','LineWidth',1)
    hold on
end

xlabel('Gate Voltage,V_G_S (V)')
ylabel('\phi_s_b_u_l_k (\bar{V})')
legend('Model' , 'Iteration',2) % 2 means top left corner, 4 means top right corner
text(0.5,0.65,'NSUB')
text(0.5,0.61,'= 10^1^5cm^-^3')
text(0.5,0.46,'= 5 x 10^1^5cm^-^3')
text(0.5,0.33,'= 10^1^6cm^-^3')
text(0.5,0.12,'= 5 x 10^1^6cm^-^3')
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% del_phi_s plot section By adding this del_phi_s with semiclassical phi_sf
% one can get QM phi_sf phi_sf_calc for different Vcb, where Nsub=1e15
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Vgs=linspace(VFB,4.5,1000); % For analytical model
Vg=Vgs-VFB; % For analytical model

Vgsi=linspace(VFB,4.5,30); % For iteration. Here few points are taken for faster computation.
Vgi=Vgsi-VFB; % For iteration. Here few points are taken for faster computation.

Nsub=1e15; % Substrated doping(or impurity in bottom silicon part) [cm^-3]
VCB=[0 1 2 3 4]; % Channel floating voltage
for i=1:length(VCB)
    Vcb=VCB(i);
    [phi_sf]=phi_calc();
    [quantum_phi_sf,del_phi_sf]=quantum_correction(Vgs,VFB,Vcb);
    % function derived in the function derivation section

    figure(6)
    plot(Vgs-VFB,abs(del_phi_sf),'k','LineWidth',2)
    hold on
end
xlabel('V_G_S-V_F_B (V)')
ylabel('\delta\phi_s_f (V)')
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%phi_sf_calc for different Vcb, where Nsub=1e15
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

for i=1:length(VCB)
    Vcb=VCB(i);
    % The following 3 functions are derived in the function derivation
    % section
    [phi_sf]=phi_calc();
    [quantum_phi_sf,del_phi_s]=quantum_correction(Vgs,VFB,Vcb);
    [phi_sf_iter,phi_sb_iter,phi_sbulk_iter,error1,error2,error3]=phi_calc_iter(Vgi,Vcb);

    figure(7)
    % Vg=Vgs-VFB; Vgi=Vgsi-VFB
    plot(Vg,abs(phi_sf),'k','LineWidth',2)
    hold on
    plot(Vgi,abs(phi_sf_iter),'+k','LineWidth',2)
    hold on
    plot(Vg,abs(quantum_phi_sf),'k','LineWidth',2)
    hold on
end

```



```

xlabel('V_G_S-V_F_B (V)')
ylabel('\phi_s_f (V)')
legend('Semiclassical Model', 'Iteration', 'Quantum Model', 2) %2 means top left corner, 4 means
% top right corner
text(3.9, 0.9, 'V_C_B = 0 V')
text(4.35, 1.9, '1 V')
text(4.35, 2.9, '2 V')
text(4.35, 3.9, '3 V')
text(4.35, 4.6, '4 V')
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Drain current calculation section.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Vgsk=[0.5, 1, 1.5, 2, 2.5]; % For analytical model
Vcb=linspace(0, 3, 30); % Channel floating voltage after eq(2) last line of 1st paragraph
for i=1:length(Vgsk)
    Vgs=Vgsk(i);
    Vg=Vgs-VFB; %after eq(10) for analytical model

    [Ids_sc, Ids_qmc]=drain_current_from_surface_potential(Vgs, VFB, Vcb);

    figure(8)
    plot(Vcb, (Ids_sc*1e6), 'k', 'LineWidth', 2)
    hold on
    plot(Vcb, (Ids_qmc*1e6), 'k', 'LineWidth', 2)
end

xlabel('Drain to Source Voltage, V_D_S (V)')
ylabel('I_D_S (\mu A)')
legend('Semiclassical Model', 'Quantum Model', 2) %2 means top left corner, 4 means top right
% corner
text(2.2, 0.9, 'V_G_S = 0.5 V')
text(2.2, 3.3, 'V_G_S = 1.0 V')
text(2.2, 5.3, 'V_G_S = 1.5 V')
text(2.2, 8.2, 'V_G_S = 2.0 V')
text(2.2, 11, 'V_G_S = 2.5 V')
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%functions definition or processing part start here
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [alpha, gamma, gamma_bulk, beta]=parameter_constant()
    % In MATLAB there is built-in alpha, beta, and gamma so be careful
    % q, esi, tsoi, Cox, Csoi, Cbox, Nch, Nsub
    alpha=(q*Nch*tsoi^2)/(2*esi); % After eq(2.9)
    gamma=sqrt(2*q*Nch*esi)/Cox; % After eq(2.5)
    gamma_bulk=sqrt(2*q*Nsub*esi)/Cbox; % After eq(2.9)
    beta=0.5*gamma_bulk*(1+(Cbox/Csoi)); % After eq(2.15)
end

function [phi_sf_weak]=phi_weak_calc(Vg)
    % q, esi, eox, tox, tsoi, tbox, Cox, Ceff, Vg, Nch, Nsub Following function
    % must called in this function: 1.parameter_constant function,
    [alpha]=parameter_constant();

    Vc=alpha+((q*Nch*tsoi)/Cox); % eq(2.11)
    Eb=(-(q*Nsub)/Ceff)+sqrt(((q*Nsub)/Ceff).^2+((2*q*Nsub)/esi)*(Vg-Vc)); % eq(2.12)
    phi_sf_weak=Vg-((esi*tox/eox)*(Eb+(q*Nch*tsoi/esi))); % eq(2.13)
end

function [phi_sf_strong_approx1, phi_sf_strong_approx2, phi_sf_strong_approx3]...
    =phi_sf_strong_approximation(Vcb)
    % eta, delta2, phi_t, phi_f, Vcb Following function must called in this
    % function: 1.phi_weak_calc function
    [phi_sf_weak]=phi_weak_calc(Vg);

    phi_sf_strong_approx1=2*phi_f+Vcb; % eq(2.16)
    phi_sf_strong_approx2=(2*phi_f+Vcb)+((phi_sf_weak-2*phi_f-Vcb)/...
        sqrt(1+((phi_sf_weak-2*phi_f-Vcb)/(eta*phi_t)).^2)); % eq(2.17)
    f=(phi_sf_weak+2*phi_f+Vcb-sqrt((phi_sf_weak-2*phi_f-Vcb).^2+4*delta2^2))/2;

```

```

% eq(2.18)
phi_sf_strong_approx3=f+((phi_sf_weak-f)/sqrt(1+((phi_sf_weak-f)/(eta*phi_t)).^2));
%eq(2.17) modified read 3 line above eq(2.18)
end

function[phi_sf_strong,phi_sb_strong,phi_sbulk_strong,phi_sf_strong1,...
    phi_sb_strong1,phi_sbulk_strong1,phi_sf_strong2,phi_sb_strong2,...
    phi_sbulk_strong2]=phi_strong_calc(Vg,Vcb)
% Cox,Cbox,phi_t,phi_f,Vg,Vcb Following functions must called in
% this function: 1.parameter_constant 2.phi_sf_strong_approximation
[alpha,gamma,gamma_bulk,beta]=parameter_constant();
[phi_sf_strong_approx1,phi_sf_strong_approx2,phi_sf_strong_approx3]...
    =phi_sf_strong_approximation(Vcb);

phi_sbulk_strong=(-beta+sqrt((beta^2)-alpha+phi_sf_strong_approx3)).^2; % eq(2.15)
phi_sb_strong=phi_sbulk_strong+gamma_bulk*sqrt(phi_sbulk_strong); % eq(2.9)
phi_sf_strong=2*phi_f+Vcb+phi_t*log(((gamma^-2*((Vg-phi_sf_strong_approx3).^...
    2-(Cbox^2/Cox^2))*(phi_sbulk_strong-phi_sb_strong).^2)-(phi_sf_strong_approx3...
    -phi_sb_strong))./(phi_t*(1-exp(-(phi_sf_strong_approx3-phi_sb_strong)...
    /phi_t))))+1); % eq(2.14)

phi_sbulk_strong1=(-beta+sqrt((beta^2)-alpha+phi_sf_strong_approx1)).^2; % eq(2.15)
phi_sb_strong1=phi_sbulk_strong1+gamma_bulk*sqrt(phi_sbulk_strong1);
% eq(2.9) phi_sbulk_strong1 used, not phi_sbulk_strong so be careful
phi_sf_strong1=2*phi_f+Vcb+phi_t*log(((gamma^-2*((Vg-phi_sf_strong_approx1).^...
    2-(Cbox^2/Cox^2))*(phi_sbulk_strong1-phi_sb_strong1).^2)-(phi_sf_strong_approx1...
    -phi_sb_strong1))./(phi_t*(1-exp(-(phi_sf_strong_approx1-phi_sb_strong1)...
    /phi_t))))+1); % eq(2.14)

phi_sbulk_strong2=(-beta+sqrt((beta^2)-alpha+phi_sf_strong_approx2)).^2; % eq(2.15)
phi_sb_strong2=phi_sbulk_strong2+gamma_bulk*sqrt(phi_sbulk_strong2);
% eq(2.9) phi_sbulk_strong2 used, not phi_sbulk_strong1 so be careful
phi_sf_strong2=2*phi_f+Vcb+phi_t*log(((gamma^-2*((Vg-phi_sf_strong_approx2).^...
    2-(Cbox^2/Cox^2))*(phi_sbulk_strong2-phi_sb_strong2).^2)-(phi_sf_strong_approx2...
    -phi_sb_strong2))./(phi_t*(1-exp(-(phi_sf_strong_approx2-phi_sb_strong2)...
    /phi_t))))+1); % eq(2.14)
end

function[phi_sf,phi_sb,phi_sbulk]=phi_calc()
% Csoi,Cbox,phi_t Here it calculate for final approximation in
% which smooth function is applied

% Following functions must called prior to its calling
% 1.parameter_constant 2.phi_strong_calc
[alpha,gamma,gamma_bulk,beta]=parameter_constant();
[phi_sf_strong]=phi_strong_calc(Vg,Vcb);

phi_sf=phi_sf_strong-phi_t*log(1+exp((phi_sf_strong-phi_sf_weak)/phi_t)); % eq(2.19)

% Solving eq(7) and eq(8) quadratic equation
a=[-b(+or-)+sqrt(b^2-4ac)]/2a
a=1;
b=(2*alpha-2*phi_sf)-(gamma_bulk*(Cbox/Csoi)+gamma_bulk)^2;
c=(alpha-phi_sf).^2;
phi_sbulk=(-b-sqrt(b.^2-4*a*c))/(2*a); % negative sign of quadratic formula works
phi_sb=phi_sbulk+gamma_bulk*sqrt(phi_sbulk); % eq(2.9)
end

function [phi_sf_iter,phi_sb_iter,phi_sbulk_iter,error1,error2,error3]...
    =phi_calc_iter(Vg,Vcb)
% Cox,Csoi,Cbox,phi_t,phi_f
[alpha,gamma,gamma_bulk]=parameter_constant();
for i=1:length(Vg)
    guess=[.4 .4 .4];
    % intial guess should be below the lowest expected value evaluated
    %by fsolve(built-in) function
    % OPTIONS = optimset('Algorithm','levenberg-marquardt'); If
    % options not used then it will use default
    % 'trust-region-dogleg' algorithm
    [result,fval,exit]=fsolve(@(z) surface_potential_iter_calc(z,Vg(i),Vcb),guess);
    phi_sf_iter(i)=result(1);
    phi_sb_iter(i)=result(2);
    phi_sbulk_iter(i)=result(3);
    %If one plot the following three then he/she can determine
    %error in numerical calculation
    error1(i)=fval(1);

```

```

    % To see how much the obtained result diverted from zero,
    % for the calculated phi_sf_iter(i)
    error2(i)=fval(2);
    % To see how much the obtained result diverted from zero,
    % for the calculated phi_sb_iter(i)
    error3(i)=fval(3);
    % To see how much the obtained result diverted from zero,
    % for the calculated phi_sbulk_iter(i)

end
clc
function surface_potential=surface_potential_iter_calc(z,Vg,Vcb)
    % ,Cox,Csoi,Cbox,alpha,gamma,gamma_bulk,phi_t,phi_f
    phisf=z(1);
    % never write phi_sf here, it cause conflict
    % with phi_calc function's phi_sf variable during Vgs vs phi_sf plot varing Vcb
    phisb=z(2);
    % never write phi_sb here, it cause conflict
    % with phi_calc function's phi_sf variable during Vgs vs phi_sf plot varing Vcb
    phisbulk=z(3);
    % never write phi_sbulk here, it cause conflict
    % with phi_calc function's phi_sf variable during Vgs vs phi_sf plot varing Vcb

    surface_potential(1)=(Vg-phisf).^2-(Cbox^2/Cox^2)*(phisbulk-phisb).^2 ...
        +gamma^2*(-phi_t*(exp(-phisf/phi_t)-exp(-phisb/phi_t))-(phisf-phisb)...
        -exp(-(2*phi_f+Vcb)/phi_t)*(phi_t*(exp(phisf/phi_t)-exp(phisb/phi_t))...
        -(phisf-phisb))); % eq(2.5) rearranged
    surface_potential(2)=phisf-phisb-alpha-(phisb-phisbulk)*(Cbox/Csoi);
    % eq(2.6) rearranged
    surface_potential(3)=phisb-phisbulk-gamma_bulk*sqrt(phisbulk);
    % eq(2.7) rearranged
end
end

function[quantum_phi_sf,del_phi_sf]=quantum_correction(Vgs,VFB,Vcb)
    [alpha,gamma,gamma_bulk,beta]=parameter_constant();
    [phi_sf]=phi_calc();
    cm=1;% [cm]
    MV=1e6;% mega volt
    zeta1= 1.23e-20;% Assumed constant
    lamda=0.61;% power of Fox
    Fox0=Cox*(Vgs-VFB-phi_sf)/eox; % eq(3.10). In our case eox=eo*eo
    E10=zeta1*((abs(Fox0)*cm)/MV).^lamda; % eq(3.8)
    del_phi_sf_1=(Cox*(Vgs-VFB-(phi_sf+gamma*sqrt(abs(phi_sf)))).*E10)./(q*eo*Fox0);
    % eq(3.7)
    Fox1=Cox*(Vgs-VFB-(phi_sf+del_phi_sf_1))/eox; % eq(3.11). In our case eox=eo*eo
    E11=zeta1*((abs(Fox1)*cm)/MV).^lamda; % eq(3.9)
    del_phi_sf=(Cox*(Vgs-VFB-(phi_sf+del_phi_sf_1+gamma...
        .*sqrt(abs(phi_sf+del_phi_sf_1)))).*E11)./(q*eo*Fox1); % eq(3.6)
    Vtr1=-0.001;
    Vtr2=0.2;
    % The following if-else based on eq (3.12)
    if (Vgs-VFB)>=Vtr1 & (Vgs-VFB)<=Vtr2
        quantum_phi_sf=phi_sf;
    else
        quantum_phi_sf=phi_sf+del_phi_sf;
    end
end
end

function [Ids_sc,Ids_qmc]=drain_current_from_surface_potential(Vgs,VFB,Vcb)

    % This function is developed based on eq(2.20) Here it is assumed
    % that Rd=Rs

    [phi_sf]=phi_calc();
    [quantum_phi_sf,del_phi_s]=quantum_correction(Vgs,VFB,Vcb);
    Cof=Cox; % matching with previous parameter

    Rd=Rs; % Rd = drain series resistance
    Vt=phi_t;
    Vth=((q*Nch*tsoi)/Cox)+VFB+2*phi_f); % Threshold voltage
    V_GST=Vgs-Vth; %Vgf-Vth
    shi_sL__shi_s0_sc=phi_sf-phi_sf(1); % For semiclassical, shi_sfL-shi_sf0
    shi_sL__shi_s0_qm=quantum_phi_sf-quantum_phi_sf(1); % For QM, shi_sfL-shi_sf0

    b1_sc=-W*Cof*mu_n*(Rs+Rd)*(V_GST+eta*Vt-(eta*Rd/(Rs+Rd))*(shi_sL__shi_s0_sc))...
```

```

    -L-(mu_n/v_sat)*(shi_sL__shi_s0_sc);
c1_sc=W*CoF*mu_n*(V_GST+eta*Vt-(eta/2)*(shi_sL__shi_s0_sc)).*(shi_sL__shi_s0_sc);

b1_qm=-W*CoF*mu_n*(Rs+Rd)*(V_GST+eta*Vt-(eta*Rd/(Rs+Rd))*(shi_sL__shi_s0_qm))...
    -L-(mu_n/v_sat)*(shi_sL__shi_s0_qm);
c1_qm=W*CoF*mu_n*(V_GST+eta*Vt-(eta/2)*(shi_sL__shi_s0_qm)).*(shi_sL__shi_s0_qm);

Ids_sc=-(c1_sc./b1_sc);
Ids_qmc=-(c1_qm./b1_qm);
end
end

```

References

- [1] J. He, X. Zhang, G. Zhang, M. Chan, and Y. Wang, "A Carrier-Based Analytic Model for Undoped (Lightly Doped) Ultra-Thin-Body Silicon-on-Insulator (UTB-SOI) MOSFETs," in *Proc. 7th Int. Conf. Quality Electronic Design*, Mar. 2006, pp. 6–12.
- [2] F. Stern, "Self-consistent results for n-type Si inversion layers," *Phys. Rev. B, Condens. Matter*, vol. 5, no. 12, pp. 4891–4899, Jun. 1972.
- [3] T. Sakurai, A. Matsuzawa, and T. Douseki, *Fully depleted SOI CMOS circuits and technology for ultra-low power applications*. Netherlands: Springer, 2006.
- [4] J. Widiez, T. Poiroux, M. Vinet, M. Mouis, and S. Deleonibus, "Experimental comparison between sub-0.1 mm ultrathin SOI single- and double- gate MOSFETs: Performance and mobility," *IEEE Trans. Nanotechnology*, vol. 5, no. 6, pp. 643–648, Nov. 2006.
- [5] H. Lim and J.G. Fossum, "Threshold voltage of thin-film Silicon-on-Insulator (SOI) MOSFETs," *IEEE Trans. Electron Devices*, vol. 30, no. 10, pp. 1244–1251, Oct. 1983.
- [6] Y. S. Yu, S. H. Kim, S. W. Hwang, and D. Ahn, "All analytic surface potential model for SOI MOSFETs," in *Proc. Inst. Elect. Eng. Circuits Devices Syst.*, vol. 152, no. 2, pp. 183–189, Apr. 2005.
- [7] J. W. Sleight and R. Rios, "A continuous compact MOSFET model for fully and partially-depleted SOI devices," *IEEE Trans. Electron Devices*, vol. 45, no. 4, pp. 821–825, Apr. 1998.
- [8] S. Bolouki, M. Maddah, A. Afzali-Kusha, and M. E. Nokali, "A unified I-V model for PD/FD SOI MOSFETs with a compact model for floating body effects," *Solid State Electron.*, vol. 47, no. 11, pp. 1909–1915, Nov. 2003.
- [9] R. Pandey and A. K. Dutta, "A Unified Analytical One-Dimensional Surface Potential Model for Partially Depleted (PD) and Fully Depleted (FD) SOI MOSFETs," *Journal of semiconductor Technol. and science*, vol. 11, no. 4, Dec. 2011.
- [10] T. L. Chen and G. Gildenblat, "Analytical approximation for the MOSFET surface potential," *Solid State Electron.*, vol. 45, no. 2, pp. 335–339, 2001.
- [11] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. V. Langevelde, G. D. J. Smit, A. J. Scholten, and D. B. M. Klassen, "PSP: An advanced surface-potential-based MOSFET model for circuit simulation," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 1979–1993, Sep. 2006.
- [12] A. R. Boothroyd, S. W. Tarasewicz, and C. Slaby, "MISNAN—A physically based continuous MOSFET model for CAD applications," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 10, no. 12, pp. 1512–1529, Dec. 1991.
- [13] *MOS-11*, NXP Semiconductors, Berlin, Germany [Online]. Available: http://www.semiconductors.philips.com/Philips_Models.

- [14] J. He, Y. Song, X. Niu, G. Zhang, M. Chan, B. Li, R. Huang, and Y. Wang, "PUNSIM: An advanced surface potential based MOSFET model," in *Proc. MIXDES*, Gdynia, Poland, Jun. 2006, pp. 111–116.
- [15] C. B. Jie, S. Z. Biao, Y. Zhong, S. Ting, and J. Zheng, "Modeling of front and back gate surface potential of deep-submicro FD-SOI MOSFET," in *Proc. 6th Int. Conf. Solid State Integr. Circuits Technol.*, 2001, vol. 2, pp. 867–870.
- [16] G. Gildenblat, X. Cai, T. L. Chen, X. Gu, and H. Wang, "Reemergence of the surface-potential-based compact MOSFET models," in *IEDM Tech. Dig.*, Dec. 2003, pp. 36.1.1–36.1.4.
- [17] G. Gildenblat, H. Wang, T. L. Chen, X. Gu, and X. Cai, "SP: An advanced surface-potential-based compact MOSFET model," *IEEE J. Solid State Circuits*, vol. 39, no. 9, pp. 1394–1406, Sep. 2004.
- [18] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 399–402, Feb. 1989.
- [19] G. F. Niu, R. M. M. Chen, and C. Ruan, "Comparisons and extension of recent surface potential models for fully depleted short-channel SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 43, no. 11, pp. 2034–2037, Nov. 1996.
- [20] N. Sadachika, D. Kitamaru, Y. Uetsuji, D. Navarro, M. M. Yusoff, T. Ezaki, H. J. Mattausch, and M. M. Mattausch, "Completely surface-potential based compact model of the fully depleted SOI MOSFET including short channel effects," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2017–2024, Sep. 2006.
- [21] P. Francis, A. Terao, D. Flandre, and F. V. de Wiele, "Modeling of ultrathin double-gate nMOS/SOI transistors," *IEEE Trans. Electron Devices*, vol. 41, no. 5, May 1994.
- [22] P. Agarwal, G. Saraswat, and M. J. Kumar, "Compact surface potential model for FD SOI MOSFET considering substrate depletion region", *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 789-795, Mar. 2008.
- [23] S. L. Jang, B. R. Huang, and J. J. Ju, "A unified analytical fully depleted and partially depleted SOI MOSFET model," *IEEE Trans. Electron Devices*, vol. 46, no. 9, pp. 1872–1876, Sep. 1999.
- [24] *BSIMSOI v2.1 MOSFET Model- user's manual for BSIM DD2.1*, University of California, Berkeley, Sep. 1999.
- [25] *BSIM-SOI 4.3.1 MOSFET Model User's Manual*, University of California, 2010.
- [26] S. K. H. Fung, P. Su, and C. Hu, "Present status and future direction of BSIM SOI model for high-Performance/Low-Power/RF application," in *Proc. Model. Simul. Microsyst.*, 2002, pp. 690–693.
- [27] S. Veeratahavan and J. G. Fossum, "A physical short-channel model for the thin-film SOI MOSFET applicable to device and circuit CAD," *IEEE Trans. Electron Devices*, vol. 35, no. 11, pp. 1866–1875, Nov. 1988.
- [28] V. Trivedi and J. G. Fossum, "Scaling fully depleted SOI CMOS," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2095–2103, Oct. 2003.
- [29] D. Kitamaru, "Development and modeling of the fully depleted SOIMOSFET model, HiSIM-SOI," Master's Degree dissertation, Hiroshima University, Hiroshima, Japan, Mar. 2003.

- [30] D. Kitamaru, Y. Uetsuji, N. Sadachika, and M. Miura-Mattausch, "Complete surface-potential-based fully-depleted silicon-on-insulator metal-oxide-semiconductor field-effect-transistor model for circuit simulation," *Jpn. J. Appl. Phys.*, vol. 43, no. 4B, pp. 2166–2169, 2004.
- [31] M. J. V. Dort, P. H. Woerlee, and A. J. Walker, "A simple model for quantisation effects in heavily-doped silicon MOSFETs at inversion conditions," *Solid State Electron*, vol. 37, no. 3, pp. 411-414, Mar. 1994.
- [32] M. A. Karim, and A. Haque, "A Physically Based Accurate Model for Quantum Mechanical Correction to the Surface Potential of Nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 2, Feb. 2010.
- [33] J. R. Brews, "A charge-sheet model of the MOSFET," *Solid State Electron*, vol. 21, no. 2, pp. 345-346, 1978.
- [34] G. Gildenblat, W. Wu, X. Li, H. Wang, G. Workman, S. Veeraraghavan, and C. McAndrew, "SP-SOI: A third generation surface potential based compact MOSFET model," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2005, pp. 819–822.
- [35] M. S. L. Lee, B. N. Tenbroek, W. Redman-White, J. Benson, and M. J. Uren, "A physically based compact model of partially depleted SOI MOSFETs for analog circuit simulation," *IEEE J. Solid State Circuits*, vol. 36, no. 1, pp. 110–121, Jan. 2001.
- [36] C. Riddet, "Monte Carlo Study of Current Variability in UTB SOI DG MOSFETs", Ph.D. thesis, University of Glasgow, 2008.
- [37] R. van Langevelde and F. M. Klaassen, "Explicit surface-potential-based MOSFET model for circuit simulation," *Solid State Electron.*, vol. 44, no. 3, pp. 409–418, 2000.
- [38] H. J. Park, P.K. Ko, and C. Hu, "A charge sheet capacitance model of short channel MOSFET's for SPICE," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 10, pp. 376–389, 1991.
- [39] Y. G. Chen, S. Y. Ma, J. B. Kuo, Z. Yu, and R. W. Dutton, "An analytical drain current model considering both electron and lattice temperatures simultaneously for deep submicron ultrathin SOI NMOS devices with self-heating," *IEEE Trans. Electron Devices*, vol. 42, no. 5, pp. 899-906, 1995.
- [40] N. D. Arora, R. Rios, and C. L. Huang, "Modeling the polysilicon depletion effect and its impact on submicrometer CMOS circuit performance," *IEEE Trans. Electron Devices*, vol. 42, no. 5, pp. 935–943, May 1995.
- [41] S. S. Chen, and J. B. Kuo, "An analytical CAD kink effect model of partially-depleted SOI NMOS devices operating in strong inversion," *Solid-State Electron.*, vol. 41, no. 3, pp. 447–458, 1997.
- [42] J. P. Colinge, J. C. Alderman, W. Xiong, and C. R. Cleavelin, "Quantum-Mechanical effects in trigate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 5, May 2006.
- [43] T. Ernst, S. Cristoloveanu, G. Ghibaudo, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, and K. Murase, "Ultimately thin double-gate SOI MOSFETs", *IEEE Trans. Electron Devices*, vol. 50, no. 3, March 2003.

- [44] F. Stern and W. E. Howard, "Properties of surface space-charge layers", *Phys. Rev.* 163, pp. 816-835, 1967.
- [45] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal oxide (insulator)-semiconductor transistors," *Solid State Electron*, vol. 9, no. 10, pp. 927-937, Oct.1966.
- [46] F. Li, S. Mudanai, L.F. Register, and S. K. Banerjee, "A physically based compact gate C-V model for ultrathin (EOT~1nm and below) gate dielectric MOS devices," *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1148-1158 Jun. 2005.
- [47] S. Mudanai, L.F. Register, A. F. Tasch, and S. K. Banerjee, "Understanding the effects of wave function penetration on the inversion layer capacitance of NMOSFETs," *IEEE Electron Device Lett.*, vol. 22, no. 3, pp. 145-147, 2001.