Effects of Interface States on MOS Gate C-V Characteristics

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Abstract

A simple gate capacitance-voltage model for MOS devices with semi-classical method is proposed. Quantum mechanical (QM) effects are neglected in the model. In this model the effects of interface trap charges are included. The model is valid for arbitrary distribution of D_{it} within the silicon energy bandgap. We have performed numerical calculation for uniform and parbolic Dit profiles. The interface trap charges are included in surface charges to calculate the oxide electric field and this oxide electric field is used to calculate the gate voltage. When we calculate the gate capacitance with these changes, a significant effect of interface trap density on C-V characteristics is observed. The doping density dependence of this effect is also studied. It is expected that the proposed model can be used for quick estimation of the effects of the interface traps on the gate capacitance-voltage characteristics.

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Authorization page

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Chapter 1

Introduction

Metal oxide semiconductor **(MOS)** transistors are the basic building blocks of MOS integrated circuits (IC). It is used in a vast manner in VLSI design for high speed performance, safe operating area, uni-polarity and ease to be used in parallel. Over the past decade, the complexity of MOS IC's has increased at an astonishing rate. This is realized mainly through the reduction of MOS transistor dimensions in addition to the improvements in processing [1].

For the study of MOSFET characteristics and operations various models have been proposed. All these models have their own assumptions and predictions. Due to scaling of MOSFETs, it has become very significant to consider the effect of generated traps in Si-SiO_2 junctions. The interface states although are not of significance in case of thicker gate oxides, but study of devices with gate oxide thickness ($\leq 2nm$) shows that these almost negligible states have remarkable impact on the drive current [2]. As the oxide thickness is reduced these interface trapped charges become significant gradually. In earlier times, gate oxide thickness was so large that this phenomenon was not noticeable, but introduction of nanotechnology has made possible MOSFETs with ultra thin oxides. As a result, now a day it is a matter of importance to consider the interface states during MOS operation.

A theoretical treatment on the process of hot electron emission from silicon into SiO_2 was carried out by Ning [3]. He considered avalanche and non-avalanche injection mechanism to calculate emission probability of the carriers at Si-SiO_2 interface. Yamabe and Miura [4] observed experimentally the flat band voltage shift due to the generation of interface states because of electron trapping in the SiO_2 film. They suggested that the interface states, where electrons can be trapped, are generated due to the collisions of electrons at the Si-SiO2 interface.

Khusru and others [5] observed that holes are created by ionizing radiation that produces new electronic states at the Si-SiO_2 interface resulting in the formation of interface traps. They also

found a threshold voltage shift due to the trapping of carriers inside the SiO_2 layer. In a recent approach, Wen and others [6] showed that the generated electron traps at the Si-SiO_2 interface enhance the degradation of MOSFET characteristics. To determine the interface trapped charges in a Si-SiO_2 interface Goreseneken and others [7] used the charge pumping method introduced by Brugler and Jespers [8] and represented a very keen analysis of energy distribution of interface trapped charges.

Effects of Interface traps can be analyzed from C-V curve characteristics. A simple semi-classical model of C-V is proposed in this work. Several simulation results are presented using this model.

1.1 Background

Generally, an interface trapped charge (also called fast interface state charge) exists at the oxide semiconductor interface. It is caused by the defects at the interface, which gives rise to charge "traps"; these can exchange mobile carriers with the semiconductor, acting as donors or acceptors [9]. The interface trapped charges are very negligible in effect in case of strong inversion but if we consider the case of very thin gate oxides then we find the trapped charges play a vital role in case of determining MOS capacitance.

The capacitance-voltage measurement helps to evaluate the flat band shift and the total interface trapped charge Q_{it}. The influence of interface traps on the biasing voltage, however, causes a shift of the ideal MOS curve along the voltage axis because, when interface traps are present, more charges on the gate are necessary to create a given surface potential. When voltage is applied, the interface trap levels move up or down with the valence and conductance bands while the Fermi level remains fixed. A change of charge in the interface trap occurs when it crosses the Fermi level. This change of charge contributes to the MOS capacitance and changes are observed in the ideal MOS capacitance curve.

Interface traps are electrically active defects with an energy distribution throughout the Si band gap which contributes to the elcetrical activity at room temperature and higher. These act as generation recombination centers and contributes to leakage current, low frequency noise and reduced mobility, drain current, and transconductance [10]. Since these traps are occupied by electrons and holes they also contribute to the threshold voltage shift which is why it is necessary to make analysis by observing the changes in the C-V characteristics.

The prime factor behind the degradation of MOS device characteristics is generation of interface traps at the Si/SiO_2 interface of metal-oxide-semiconductor (MOS) structures. At low frequency C-V characteristic curve depends on the distribution of the density of interface trap states (D_{it}) states within Si band gap even for the same average value of D_{it} [11]. It is required to have the knowledge of the density of interface trap states (D_{it}) throughout the band gap, rather than the average density of states at midgap. Characterization of the interface traps has been an important task for accurate estimation of device life-time reliability.

1.2 Objective of This Work

Gate capacitance voltage measurements of MOS capacitor structures provide a wealth of information about the structure which is of direct interest when one evaluates an MOS process. Since the MOS structure is simple to fabricate the technique is widely used.

As mentioned earlier, for accurate estimation of device life time reliability, characterization of interface traps is an important task. There are several techniques for extracting interface trap states, such as, charge pumping method [12], conductance method [13], Terman method [14], low frequency C-V method [15] and combined low-frequency/high frequency C-V method [16]. In this work, we propose a semi-classical model for gate C-V characteristics including interface trap charge. Interface trap charge Q_{it} is calculated and included in the C-V curve. Using this model several simulations are done with and without D_{it} distribution to study the non-ideal effects caused by the presence of traps and its effects on C-V characteristics of MOS gate capacitance. To keep the model simple and computationally efficient, quantum-mechanical (QM) effects are neglected in this study.

1.3 Organization of The Thesis

In chapter 2 necessry review of MOSFET and interface states are given. In the following chapter 3, theory to develop C-V characteristics and detailed calculation of interface trap charge is stated. Verification and comparison of simulated C-V including trap charge density is presented in chapter 4. Summary and future work is presented in conclution in chapter 5. Flowchart of our work is given in the appendix section.

Chapter 2

Review of Basic MOS Theory

The $Si\text{-}SiO_2$ interface perfection has been the reason why MOSFET devices are suitable for many applications. Their higher areal density, better switching characteristics and lower power dissipation have made them the dominant device in electronic systems and the engine driving Moore's law [17]. To understand the operation of the MOSFET we first need to examine the MOS capacitor, whose structure, band diagrams and its four different modes of operation are shown in this chapter. We have also discussed the gate capacitance and interface states in detail with band diagrams.

2.1 MOSFET Basics

MOSFET is an electronic device which is widely used, especially in digital integrated circuits. Silicon is used as semiconductor to make such devices, for insulator we used SiO_2, and as gate electrode heavily doped poly crystalline silicon, which is known as polysilicon or metal are widely used. To refer this devices the term *metal oxide semiconductor field- effect transistor (MOSFET)* is generally used.

2.1.1 MOS Structure

Here we consider the n-channel enhancement-type transistor shown in Fig. 2.1. On a p-type substrate the transistor is fabricated. In the figure two heavily doped n-type regions shown as n^+ **source** and n^+ **drain** regions, are created in the substrate. Drain and Source connection are made to higher conduction high doped region. A thin layer of silicon dioxide (SiO_2) is grown on the surface of the substrate. SiO_2 is known as an excellent electrical insulator. On top of the oxide layer metal is deposited which form the **gate electrode** of the device. The metal gate is electrically isolated from p-type substrate by a layer of non-conducting SiO_2. Metal contacts are also made to the source region, the drain region, and the substrate also known as the **body**. So,

four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate body terminal (B).

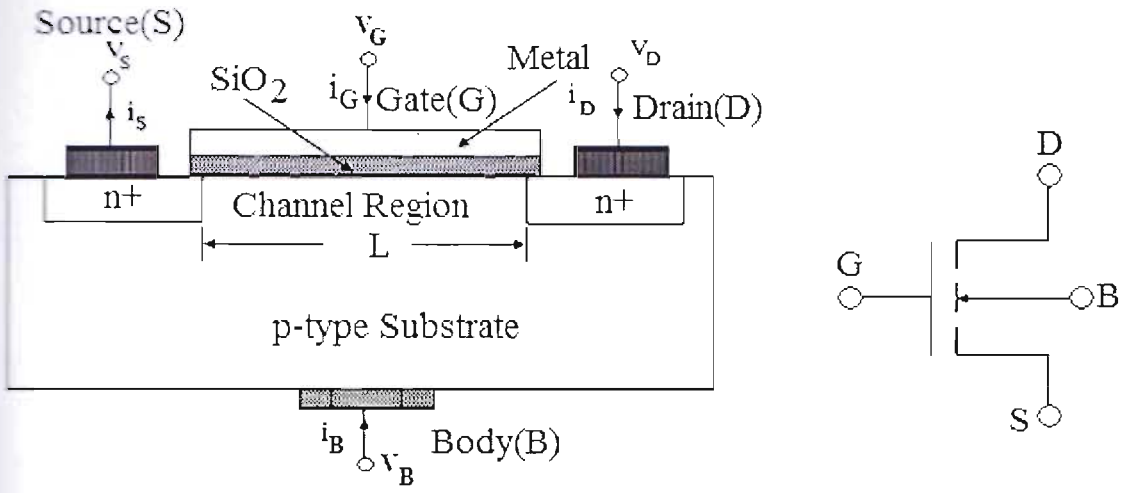


Figure 2.1: Cross section of an enhancement-type n-MOSFET.

2.1.2 Energy Band Diagram of an MOS Capacitor

The energy band diagram contains the electron energy levels in the MOS structure as delineated with the Fermi energy in the metal and semiconductor as well as the conduction and valence band edge in the oxide and the silicon. We will distinguish between four modes of operation: flat band, accumulation, depletion and inversion.

Flat band condition

Flat band conditions exist when no charge is present in the semiconductor so that the silicon energy band is flat. The flat band voltage is obtained when the applied gate voltage equals the work function difference between the gate metal and the semiconductor. However there is also a fixed charge in the oxide and/or at the oxide-silicon interface. At flat band condition $\varphi_S = 0$. The energy band diagram of an n-MOSFET at flat band is shown in Fig. 2.2.

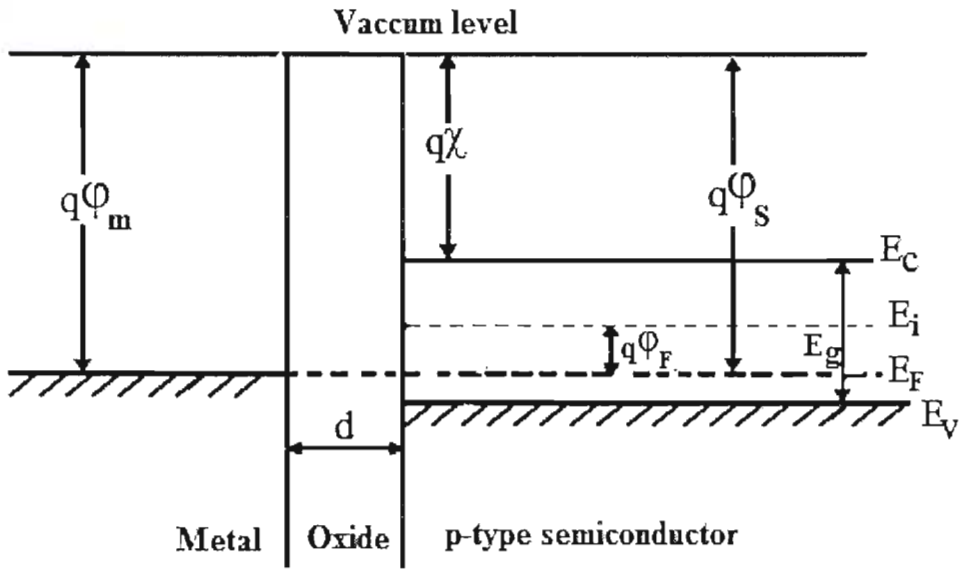


Figure 2.2: Energy band diagram of an enhancement-type n-MOSFET at flat band.

Accumulation

If a negative bias is applied between the metal and the semiconductor, the valence bands are bent to come closer to the Fermi level, causing an accumulation of holes at the interface as shown in figure 2.3. The difference between the Fermi level in the metal and the semiconductor is the applied bias.

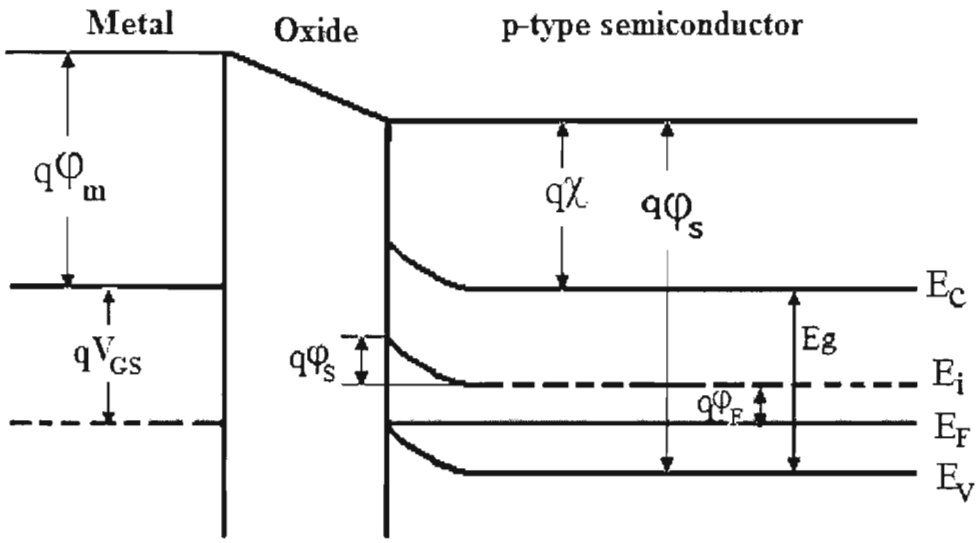


Figure 2.3: Energy band diagram of an enhancement-type n-MOSFET in Accumulation.

Surface depletion

Surface depletion occurs when a positive bias is applied to the metal with respect to the semiconductor, the Fermi level in the metal is lowered by an amount eV with respect to the semiconductor, causing the valence band to move away from the semiconductor Fermi level near the interface. As a result the hole density near the interface falls below the bulk value in the p-type semiconductor as shown in figure 2.4. Here when $\varphi_S > 0$, we have depletion region.

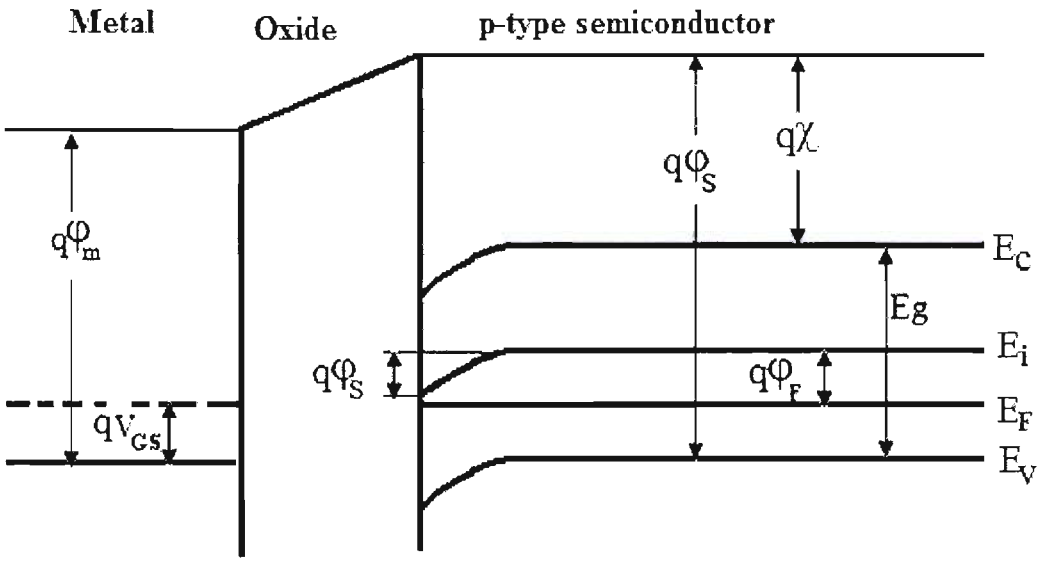


Figure 2.4: Energy band diagram of an enhancement-type n-MOSFET in Depletion.

Inversion

A more positive voltage also attracts electrons (the minority carriers) to the surface which forms the so-called inversion layer. If we increase the gate voltage the depletion layer width barely increases further since the charge in the inversion layer increases exponentially with the surface potential. Inversion occurs at more positive voltages which are larger than the threshold voltage. When φ_S is positive and larger than φ_F the bands at the surface are bent down such that E_i lies below E_F, and inversion is obtained. For strong inversion the surface should be strongly n-type as the substrate is p-type. It means that, E_i should lie as far as below E_F at the surface as it is above

E_F far from the surface. This condition occurs when $\varphi_S(\text{inv.}) = 2\varphi_F$. The energy band diagram of an n-MOSFET in inversion is shown in Fig. 2.5.

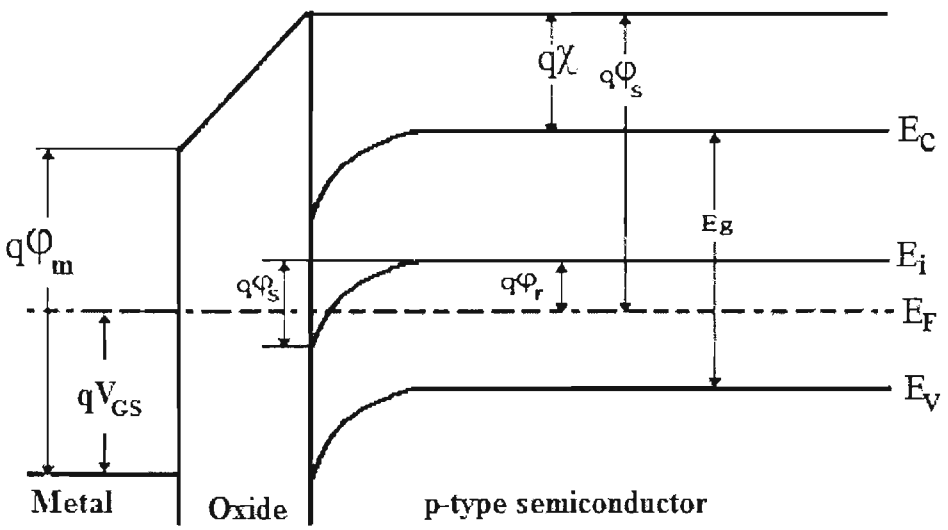


Figure 2.5: Energy band diagram of an enhancement-type n-MOSFET in strong Inversion.

2.1.3 Gate Capacitance

A voltage dependent semiconductor capacitance in series with a fixed voltage independent gate insulator capacitance is the electrical representation of a MOS capacitor. In accumulation the insulator capacitance (C_i) represents the series capacitance. When we apply negative voltage at surface holes are accumulated and the MOS appears like a parallel-plate capacitor, dominated by the insulator properties. As the voltage is less negative the semiconductor surface is depleted. The depletion capacitance (C_d) added in series with (C_i) in depletion, which gives small capacitance and the value decreases until inversion is achieved. The depletion capacitance when added with the insulator capacitance the total capacitance is small. Now the semiconductor capacitance is very large because inversion charge increases exponentially with F_S. The low frequency MOS capacitance in strong inversion is basically again (C_i). The C-V characteristic of the MOS structure depending on the conditions of semiconductor surface is in accumulation, depletion or inversion shown in Fig. 2.6.

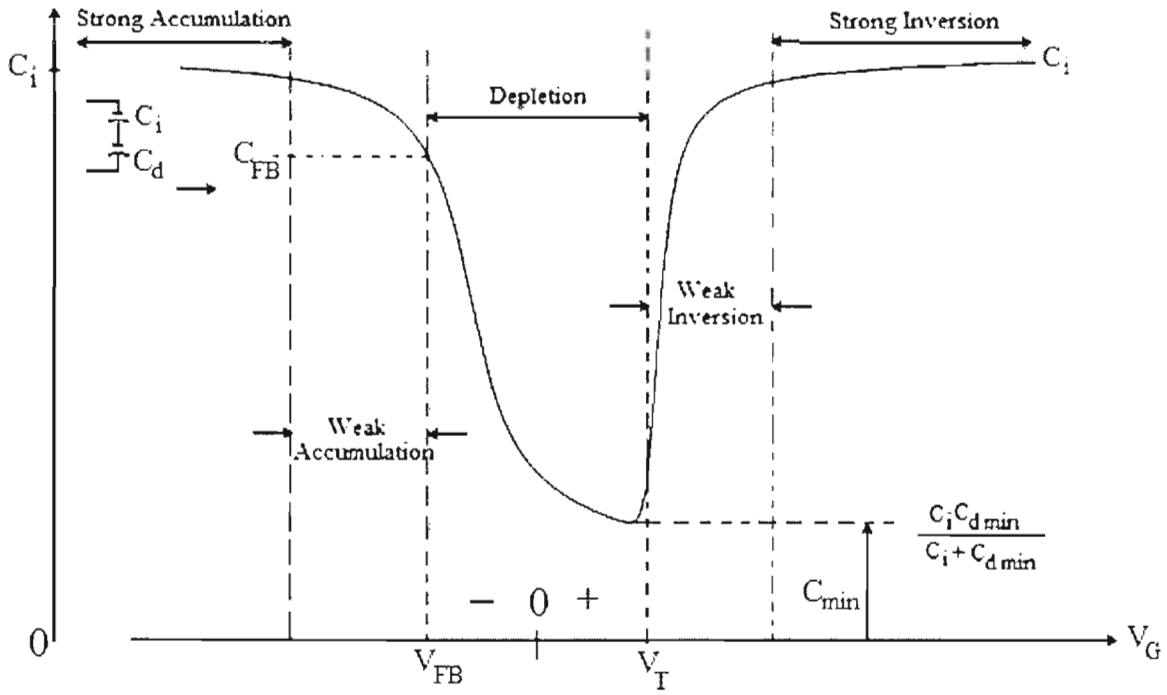


Figure 2.6: Gate C-V characteristics of an enhancement-type n-MOS.

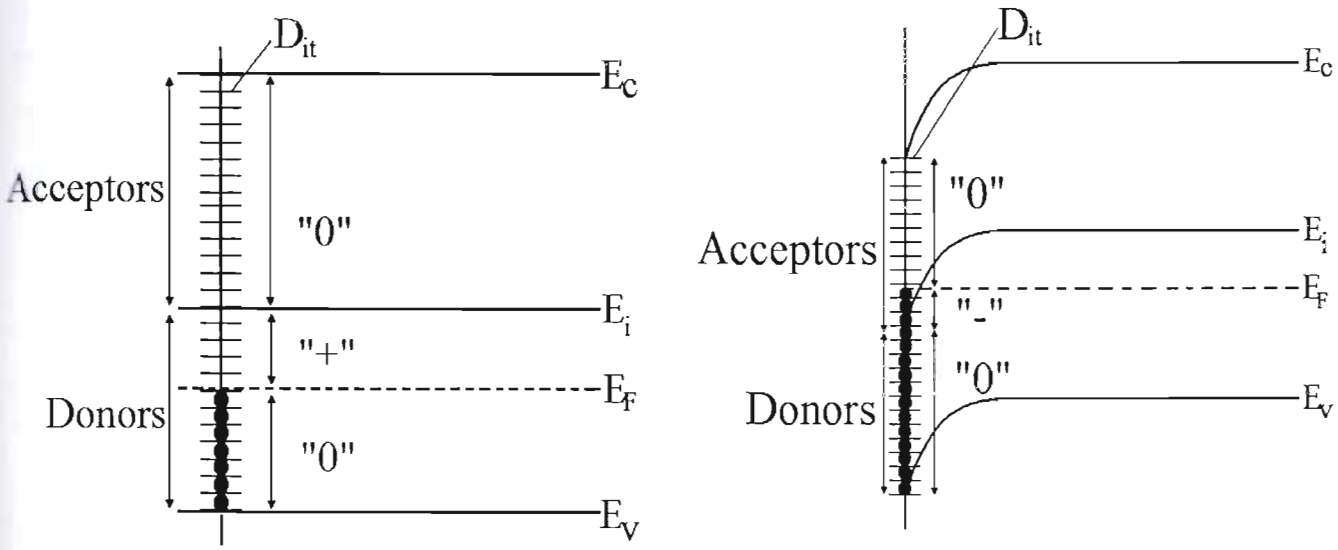
2.2 Interface States

Interface states occurs due to interface trap charges which are atoms from the silicon that remain bonded only to three silicon atoms with the fourth bond unsaturated, representing interface defects. Every trivalent silicon atom introduces a pair of energy levels; One can be occupied by an electron (acceptor type) and the other can be occupied by a hole (donor type). Electrons and holes that appear on these levels cannot move freely as there is a relatively large distance between the neighboring interfacial trivalent silicon atoms (these levels are localized and isolated from each other). As these levels can effectively trap the mobile electrons and holes (from the conduction and valence bands respectively), these are called interface states. Impurity atoms and groups (such as H, OH and N) can be bonded to the unsaturated bonds of the interfacial trivalent silicon atoms, which result in a shift of the corresponding energy levels into the conduction and valence band.

Interface states at the Si/SiO_2 in a metal-oxide-semiconductor structure play a crucial role in determining the electrical characteristics of MOSFETs [18], which include the threshold voltage (V_T), the channel carrier mobility (μ), the transconductance (gm), and the sub threshold slope (S). Accurate characterization of interface states throughout the band gap is, therefore, very important for improving the robustness of devices and their integrated circuits with MOS capacitors and MOSFETs. Interface states induce a stretching of the C-V curve, because the trap charge density depends on the Fermi level at the Si/SiO_2 and consequently on the applied gate voltage. Interface trap charge (Q_{it}) is positively or negatively charged. These are located within the silicon forbidden gap at the $Si\text{-}SiO_2$ interface. Unlike a fixed oxide charge, an interface trapped charge interacts strongly with the underlying silicon and can thus be charged or discharged, depending on the surface potential. These types of charges are also called surface states [16], fast states [19], and interface states [20].

There has been a long debate on whether the interface trap (or interface state) is acceptor or donor-like. The interface traps are generally classified as donor like (positive when empty) or acceptor-like (negative when filled with electrons). Ma and Knoll have suggested that the interface traps in the upper half of the silicon band gaps are acceptor-like and those in the lower half are donor-like [21 and 22]. Gray and Brown originally proposed this distribution and claimed that the density and distribution of acceptor traps and donor traps in the silicon band gap are almost symmetrical [20].

Interface traps at the SiO2 /Si interface are acceptor-like in the upper half and donor-like in the lower half of the bandgap. This is in contrast to doping atoms, which are donors in the upper half and acceptors in the lower half of the bandgap. Hence, as shown in Fig. 2.7(a), at flatband, where electrons occupy states below the Fermi energy, the states below the Fermi level are neutral (designated by ''0''), being occupied donor states. Those between mid gap and the Fermi energy are positively charged (designated by ''+''), being unoccupied donor states and those above E_i



(a) (b)

Fig. 2.7: Energy band diagram of *n*-channel MOSFET showing interface traps: (a) Positive interface trap charge at flatband. (b) At inversion interface traps are negatively charged. [10]

are neutral (unoccupied acceptors). For n-channel MOSFET at inversion, shown in Fig. 2.7(b), the fraction of interface traps between midgap and the Fermi level is now occupied donors, leading to negatively charged interface traps (designated by ''-''). Hence interface traps in n-channel devices in inversion are negatively charged, leading to positive threshold voltage shifts. [10]

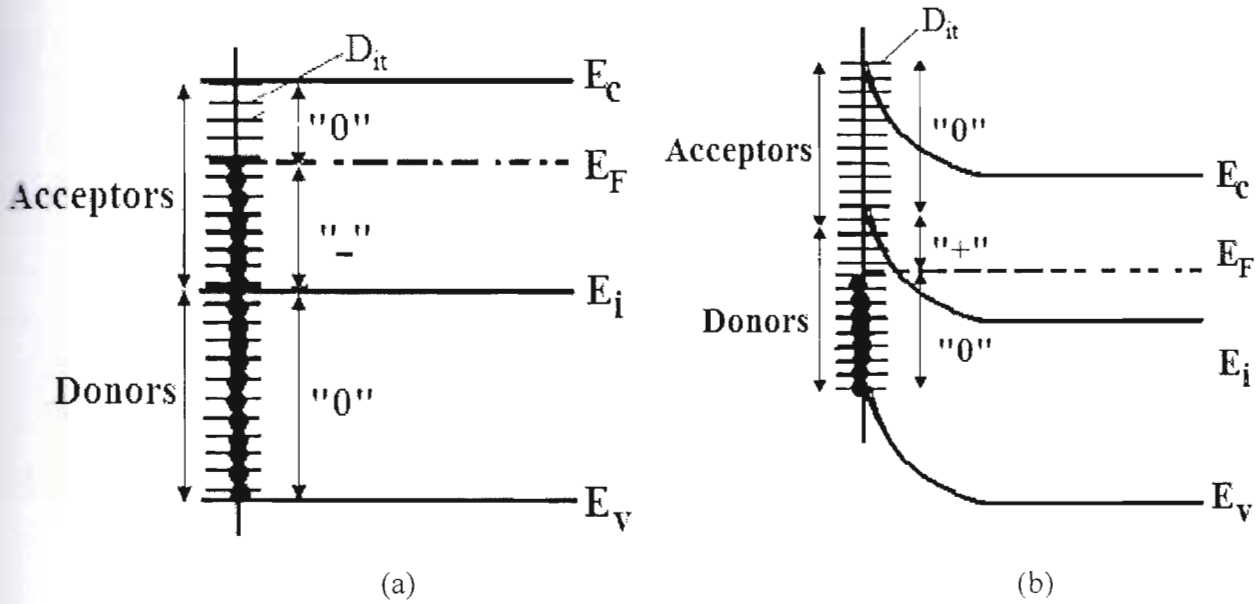


Fig. 2.8: Energy band diagram of *p*-channel MOSFET showing interface traps: (a) Negative interface trap charge at flatband. (b) At inversion interface traps are positively charged. [10]

For a p-channel MOSFET, shown in Fig. 2.8(a), at flatband, where electrons occupy states below the Fermi energy, the states in the lower half of the band gap are neutral (designated by ''0''), being occupied donor states. Those between mid gap and the Fermi energy are negatively charged (designated by ''-''), being occupied acceptor states and those above E_F are neutral (unoccupied acceptors). For an inverted *p*-channel MOSFET, shown in Fig. 2.8(b), the fraction of interface traps between mid gap and the Fermi level is now unoccupied donors, leading to positively charged interface traps (designated by ''+''). Hence interface traps in *p*-channel devices in inversion are positively charged, leading to negative threshold voltage shifts.

Chapter 3

Theory

In order to evaluate correct C-V curve for MOS device, it is necessary to extract the surface perpendicular electric field, semiconductor charge density, flat band voltage, the potential drop across the oxide, gate capacitance and interface trap charge accurately. For this we have used the following techniques in this chapter.

3.1 Poisson's Equation

Among the three operation regions mentioned in chapter 2, inversion is the most important operation region. The surface is inverted whenever φ_S is larger than φ_F, a practical criterion is needed to tell us whether a true n-type conducting channel exist in the surface [23]. For strong inversion the best criterion is that the surface should be as strongly n-type as the substrate is p-type. So that E_i should lie as far below E_F at the surface as it is above E_F far from the surface. This condition occurs when

$$\varphi_S(inv.) = 2\varphi_F = 2\frac{kT}{q} ln\frac{N_a}{n_i} \tag{3.1}$$

We now solve Poisson's equation for the MOS capacitor. Whereas most of the derivation is applicable for both n-type and p-type substrates, the equations are written in a form which is more convenient for p-type substrates, but can easily be rewritten for n-type substrates.

The total charge density, ρ, in the semiconductor is given by:

$$\rho(x) = q(\, p(x) - n(x) - N_A^- + N_D^+ \,) \tag{3.2}$$

From 1D Poisson equation we get,

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho(x)}{\varepsilon_S} \tag{3.3}$$

For p-type substrate $N_D = 0$. Now, replacing the value of ρ, from equation 3.3 we get,

$$\frac{d\varphi}{dx}\left(\frac{d\varphi}{dx}\right) = -\frac{q}{\varepsilon_S}(p(x) - n(x) - N_A) \tag{3.4}$$

Assuming the total integrated charge per unit area, Q_S, as a function of the surface potential, φ_S, Poisson's equation takes the following form:

$$\int_0^{\varphi} \frac{\partial\varphi}{\partial x}\, d\left(\frac{\partial\varphi}{\partial x}\right) = -\frac{q}{\varepsilon_S}\int_0^{\varphi}(p(\varphi) - n(\varphi) - N_A)\, d\varphi \tag{3.5}$$

A particularly important case is at the surface (x = 0) where the surface perpendicular electric field, $\xi_S = -\frac{d\varphi}{dx}$, becomes

$$\xi_S = \frac{\sqrt{2}kT}{qL_D}\left[\left(e^{-\frac{q\varphi_S}{kT}} + \frac{q\varphi_S}{kT} - 1\right) + \frac{n_0^{\,2}}{p_0^{\,2}}\left(e^{\frac{q\varphi_S}{kT}} - \frac{q\varphi_S}{kT} - 1\right)\right]^{\frac{1}{2}} \tag{3.6}$$

Where L_D, is the Debye screening length,

$$L_D = \sqrt{\frac{\varepsilon_S kT}{q^2 p_0}} \tag{3.7}$$

By using Gauss's law at the surface, we can relate the integrated space charge per unit area to the electric displacement, keeping in mind that the electric field in the substrate is zero.

$$Q_S = \varepsilon_S \xi_S \tag{3.8}$$

Electric field at oxide (ξ_{ox}) can be calculated with the analytical expression.

$$\xi_{ox} = \frac{Q_S}{\varepsilon_{ox}} \tag{3.9}$$

Now, potential drop across oxide (φ_{ox}) can be calculated using ξ_{ox} ,

$$\varphi_{ox} = \xi_{ox} t_{ox} \tag{3.10}$$

Now the substrate is affected when the externally applied voltage V_g assumes values different from the flat band voltage V_{FB}.

We can write:

$$V_g = \varphi_{ox} + \varphi_S + V_{FB} \tag{3.11}$$

The capacitance-voltage characteristics of this ideal MOS structure vary depending on whether the semiconductor surface is in accumulation, depletion or inversion. The voltage-dependent MOS gate capacitance is, [24]

$$C_g = \frac{dQ_g}{dV_g} \tag{3.12}$$

3.2 Including D_{it} effect on C-V Characteristics

It is well known that the interface traps at the Si–SiO_2 interface in the MOS structures play an important role in determining several characteristics of MOS devices. In recent years there has been an increased interest to find an accurate modeling and characterization of interface traps through the band gap, mostly using capacitance, conductance and charge pumping methods [16, 25, 26, 27]. Interface traps are now the most important non-ideality found in MOS structures Interface trap charge is evaluated by

$$Q_{it} = q \int_{E_i}^{E_C} F(E).D_{it}(E)\,dE \tag{3.13}$$

Where D_{it} is the interface trap charge density per cm^2 per eV and E is the energy level in the band gap of the semiconductor, corresponding to D_{it} (E). F(E) is Fermi-dirac distribution. Here D_{it} is arbitrarily distributed between valance energy and conduction energy level. F(E) may be approximated by its zero temperature distribution as a step function. As interface trap charge Q_{it} is effective in between Fermi energy level and intrinsic energy level we can get Q_{it} by writing equation (3.13) as,

$$Q_{it} = q \int_{E_F}^{E_i} D_{it}(E).dE \tag{3.14}$$

We have considered this Q_{it} in the calculation of oxide electric field. These charges are interrupting the electric field which comes from gate to body for positive applied voltage and body to gate for negative applied voltage. That is why the electric field has changed in the equation (3.9).

$$\xi_{ox} = \frac{Q_S - Q_{it}}{\varepsilon_{ox}} \tag{3.15}$$

Now after Q_{it} consideration the voltage-dependent semiconductor gate capacitance is calculated as,

$$C_g = \frac{d(Q_S + Q_{it})}{dV_g} \tag{3.16}$$

We have considered φ_s as an independent parameter. We calculate Q_S analytically using equation (3.6) and (3.8). Then we calculate the changed oxide electric field (ξ_{ox}) with the equation (3.15). This changed ξ_{ox} is used to calculate the potential drop across the oxide (φ_{ox}). This changed ξ_{ox} also participates to calculate gate voltage V_g in equation (3.11). Interface trap charge is calculated using the equation (3.14). Finally, we numerically evaluate the derivative of equation (3.16) using finite difference method to determine C_g.

When we consider D_{it} effects, C-V characteristics curve shape is changed and the capacitance value C_g is increased for D_{it} effects. The value of capacitance is very important in determining performance of a MOSFET. Considering the impact of D_{it} on C-V curve we proposed a model for any arbitrary D_{it} profile. For Si-SiO_2 interfaces, the most common $D_{it}(E)$ profile is parabolic centered at the mid-gap energy.

Chapter 4

Simulation and Results

In this chapter, the accuracy of our simulation will be justified by comparing the simulation result with the published simulation result. The C-V characteristics from simulation results will be discussed next. Then we observe the effects of D_{it} profiles within the energy bandgap on C-V characteristics for various doping densities. In our simulation, we have considered the distribution of D_{it} within the energy bandgap with uniform and parabolic distributions.

4.1 Verification

4.1.1 Charge Density vs. Surface Potential

Considering the parameters from [23] we have calculated the charge density (Q_S) as a function of the surface potential (φ_s). Equation (3.8) is used to calculate Q_S and the results are presented in Fig. 4.1. Here we consider an n-channel MOSFET with uniform substrate doping density of N_a = 4 x 10^{15} cm^{-3} at room temperature (300 K). Comparing our simulation with published simulated results, we verify the accuracy of our calculation.

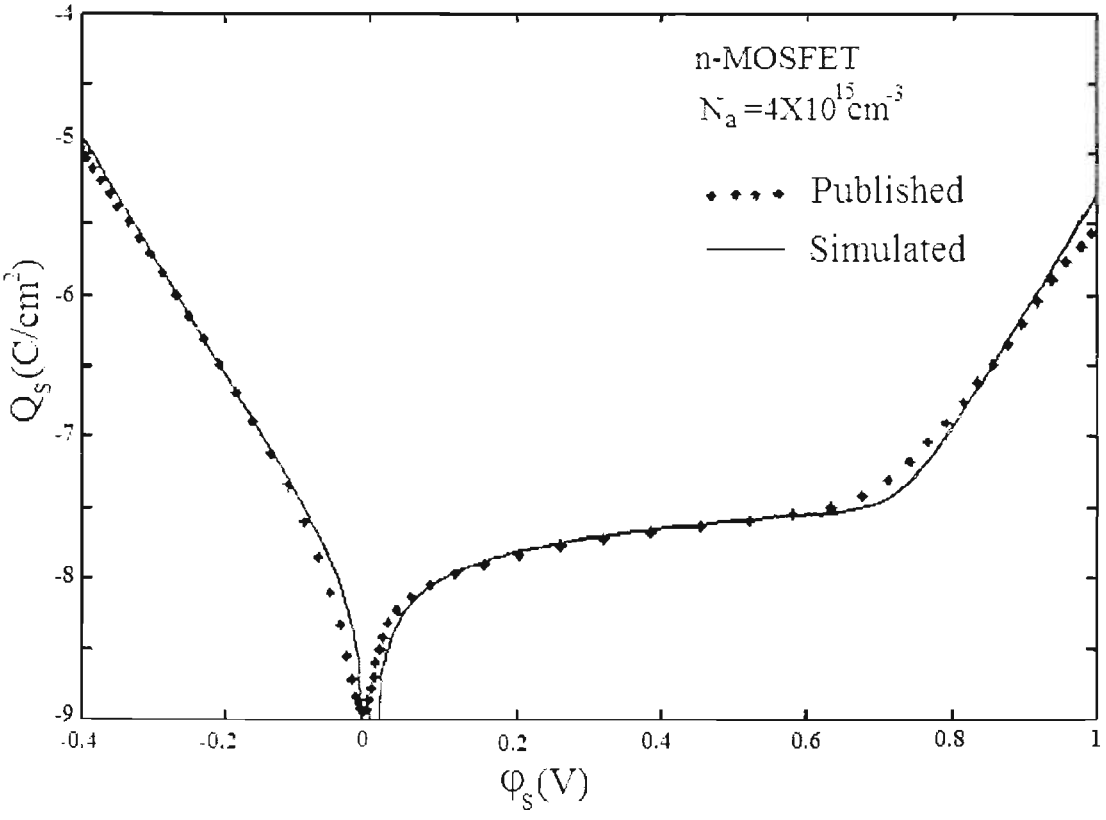


Figure 4.1: Variation of space-charge density (Q_S) in the semiconductor as a function of the surface potential (φ_s) for p-type silicon at room temperature (300 K). Published data is from [23]

Fig. 4.2 shows surface potential (φ_s) as a function of gate voltage (V_g) calculated using our model. This figure demonstrates the surface potential in both accumulation and inversion regions. Here we consider two doping density sets of n-channel MOSFETs with uniform substrate doping density of N_a = 4 x 10^{15} cm^{-3} and N_a = 6 x 10^{17} cm^{-3} keeping the same oxide thickness value t_{ox} = 3nm. In both case we keep our flat band voltage fixed (V_{FB} = -1V). The results are consistent with the known trends of the $\varphi_s - V_g$ relationship.

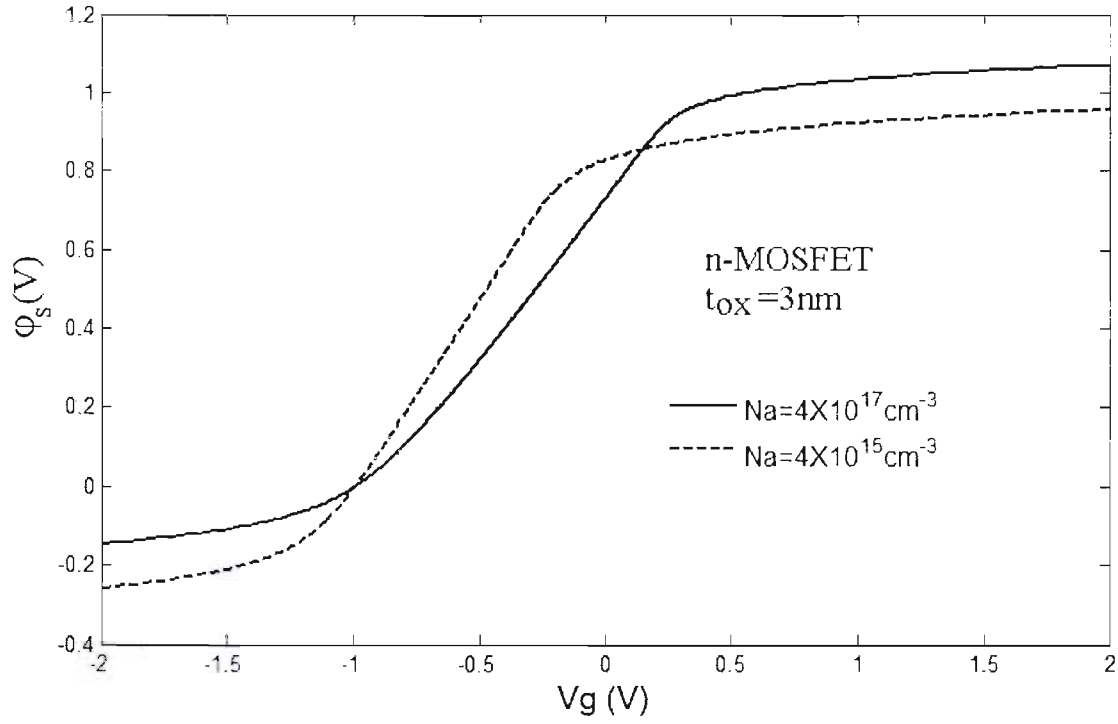


Figure 4.2: Surface potential (φ_s) as a function of gate voltage (V_g).

4.1.2 Gate capacitance vs. gate voltage

A MOS capacitor or MOSFET is the series combination of a fixed, voltage-independent gate oxide (insulator) capacitance and voltage-dependent semiconductor capacitance. The capacitance-voltage (C-V) measurements give the most detailed picture of the electrical characteristics of the Si/SiO_2 interface states. Here the semiconductor capacitance itself can be determined from the slope of the Q_S versus φ_s plot (Fig. 4.1). Two sets of n-channel MOSFETs are considered here. In both simulations we took flat band voltage V_{FB} = - 1V. The first one (Fig. 4.3) with substrate doping density of $N_a = 1 \times 10^{18}$ cm^{-3} and the oxide thickness value t_{ox} = 2 nm. Another (Fig. 4.4) is for substrate doping density of $N_a = 6 \times 10^{17}$ cm^{-3} and the oxide thickness value t_{ox} = 3 nm. These parameters are taken from a published paper [28]. Both our simulated and the published simulated results are matched which confirms that our results are correct.

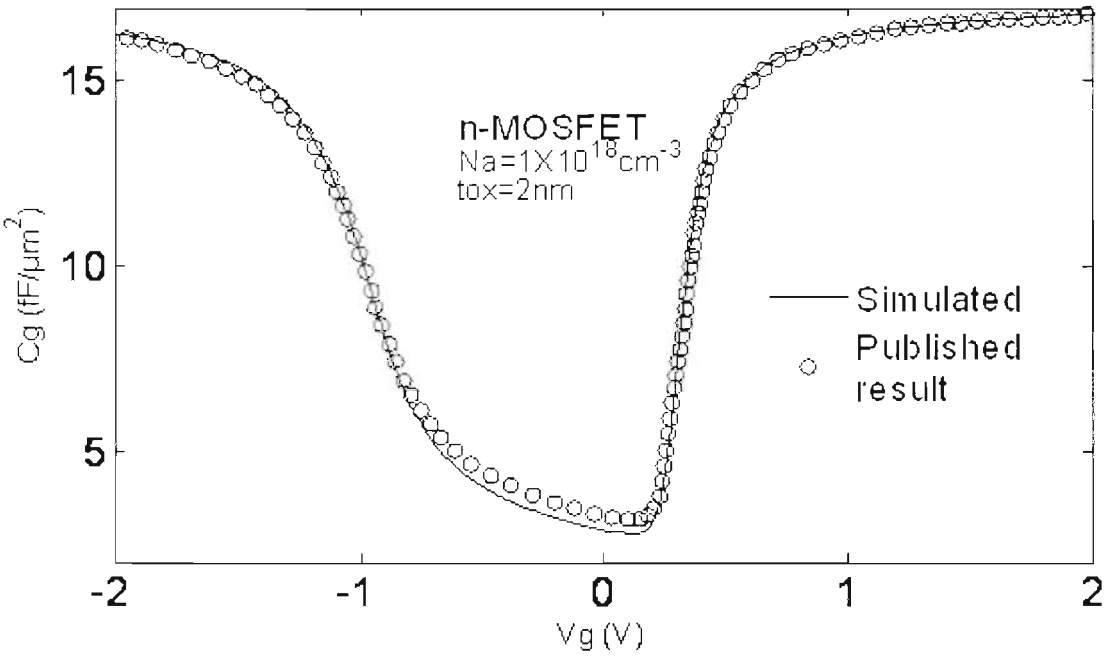


Figure 4.3: C-V characteristics for an n-channel (p-substrate) MOS capacitor with N_a = 1 x 10^{18} cm^{-3} and t_{ox} = 2nm. Published simulation data is from [28]

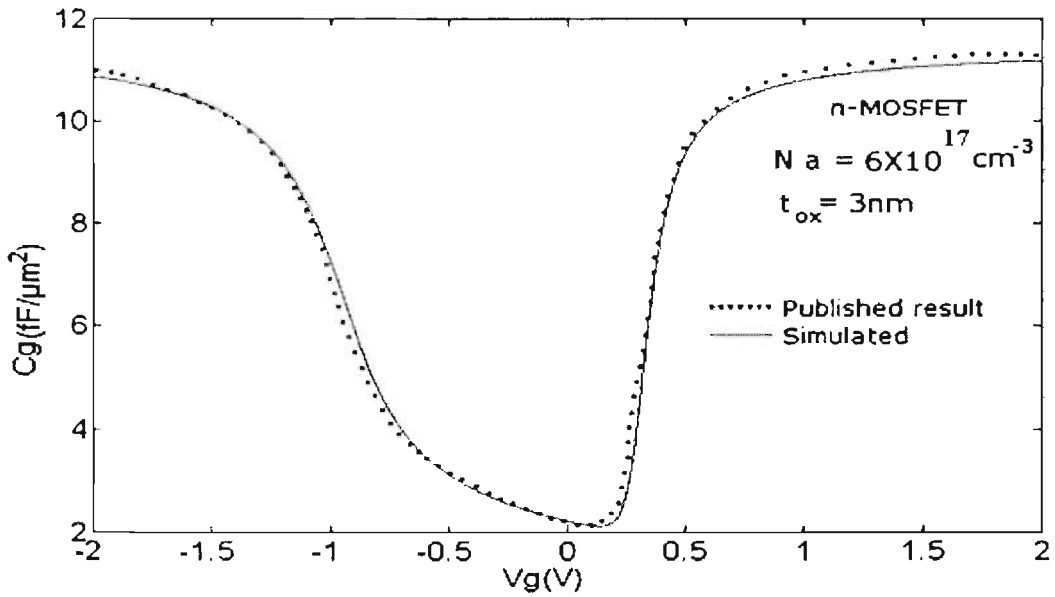


Figure 4.4: C-V characteristics for an n-channel (p-substrate) MOS capacitor with N_a = 6 x 10^{17} cm^{-3} and t_{ox} = 3nm. Published simulation data is from [28]

4.2 Effects of D_{it} on C-V characteristics

The effects of D_{it} are presented in this section. Here the low frequency gate C-V characteristics of MOSFETs are simulated assuming certain distribution of interface trap states.

4.2.1 Effects of Uniform D_{it} and Non uniform D_{it}

We observe the effect of D_{it} on gate C-V curves for various doping density. In our simulation, we have considered uniform and non-uniform distributions of D_{it}. For non-uniform case, we consider the parabolic shape. D_{it} is assumed to have donor like states below the charge neutrality level E_i and acceptor like states above it. When we take parabolic D_{it} distribution, we consider that minimum value of that distribution is at E_i.

As shown in figure 4.5 we consider the substrate doping density of 5 x 10^{17} cm^{-3} for p type Si and the oxide thickness t_{ox} = 3 nm. With the four different uniform D_{it} profile, C-V curves are simulated.

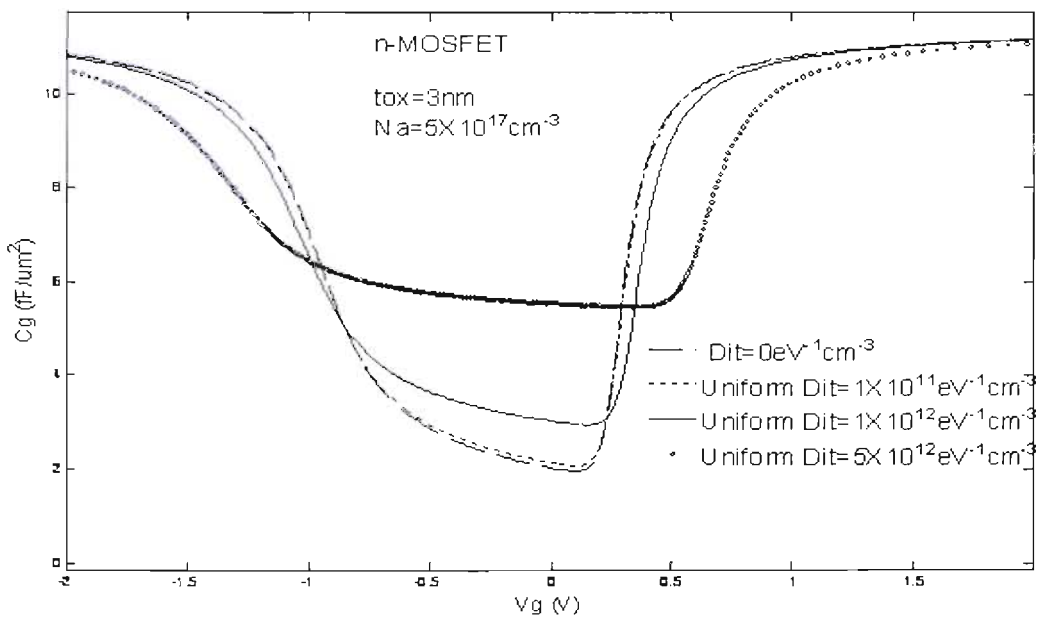


Figure 4.5: C_g versus V_g curve for SiO_2/Si MOS structure without and with uniform D_{it} profile.

Now if we observe the figure, the C-V curve is changing with the change of D_{it} profile. With the increase of D_{it}, the curve is spreading and shifting upward in depletion. It is very clear that the value of C_g is increasing as well as decreasing at different regions. If we observe carefully, in both accumulation and inversion region capacitance is decreasing but at the depletion it is increasing. This is because at depletion region due to increase of D_{it}, electric field at oxide is increasing and more surface charge is induced. Q_S decreases in depletion but increases in inversion.

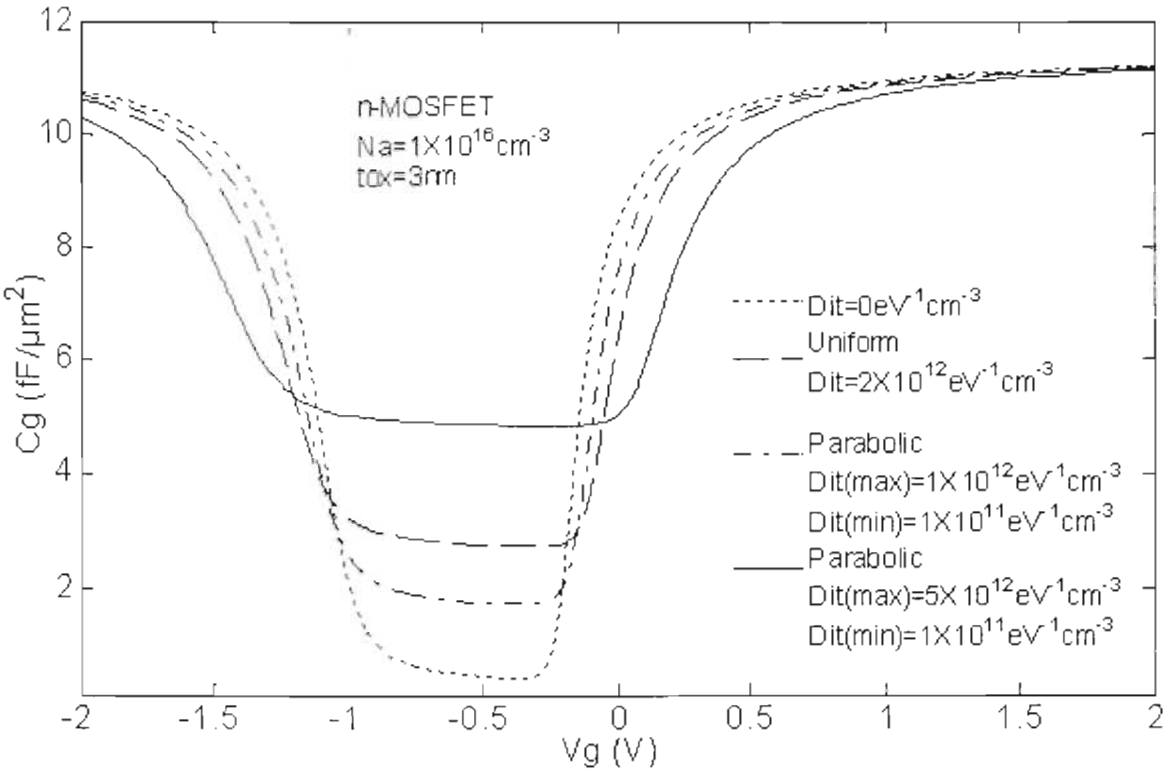


Fig. 4.6: C_g versus V_g curve for SiO_2/Si MOS structure without D_{it}, with uniform D_{it} and parabolic D_{it} profile.

Here we consider in Fig. (4.6) the substrate doping density of 1 x 10^{16} cm^{-3} for p type Si and the oxide thickness t_{ox} = 3 nm. We considered here one uniform D_{it} profile of 2 x 10^{12} eV^{-1} cm^{-2} and two non uniform D_{it} (parabolic) profiles of $D_{it(max)}$ =1 x 10^{12} eV^{-1} cm^{-2} and $D_{it(min)}$= 1 x 10^{11} eV^{-1} cm^{-1} and for another non uniform profile $D_{it(max)}$ =5 x 10^{12} eV^{-1} cm^{-2} and $D_{it(min)}$= 1 x 10^{11} eV^{-1}

cm^{-1}. In all of our calculations we consider V_{FB}= -1 V. Now if we look into this figure, the C-V curve is changing when we consider the D_{it} profile (both uniform and non uniform). First when we compare the C-V curve with D_{it} profile with ideal (without D_{it}) C-V curve, we observe that the minimum value of C_g is changed. This minimum value of C_g is around 1.2 fF/μm^2 for the ideal condition and the minimum value of C_g is around 3 fF/μm^2 for uniform D_{it}, and 2 fF/μm^2 for non uniform (parabolic) D_{it} (max=$1x10^{12}$, min=$1x10^{11}$) and 5 fF/μm^2 for non uniform (parabolic) D_{it} (max=$5x10^{12}$, min=$1x10^{11}$). This is because the interface trap charges are in between the Si-SiO_2 interface. These charges are interrupting the electric field which comes from gate to body for positive applied voltage and body to gate for negative applied voltage. That is why the electric field has changed with the equation (3.14). This changed electric field also participates to change the gate voltage, V_g. For this, the second change occurs in the C-V curve when we consider D_{it} when compared with ideal C-V curve. That is why the value of C_g starts to fall at more negative voltage and starts to rise with higher voltage. For that, the curve (non ideal) spreads towards the voltage sides. Its mean, this D_{it} increases the region of depletion and weak inversion. From the figure it is very much clear that the amount of spreading of the C-V curve is depending on the amount of D_{it}. It has major effect in the region of depletion and weak inversion and a very negligible effect in the region of accumulation and strong inversion. From both second and third changes we can say that if the doping density is higher, the C-V curve is spreading towards the voltage and starts to affect the C-V curve from more accumulation region and more strong inversion region which will be no longer negligible or small. From all of the above discussion we can strongly say that if parameters like N_a, t_{ox}, temperature etc remain constant the change of capacitance with respect to gate voltage is directly proportional to the trap charges. For more trap charges, more wide range of voltage is required to change the capacitance, and for less trap charges, less range of voltage will be needed to change the C_g.

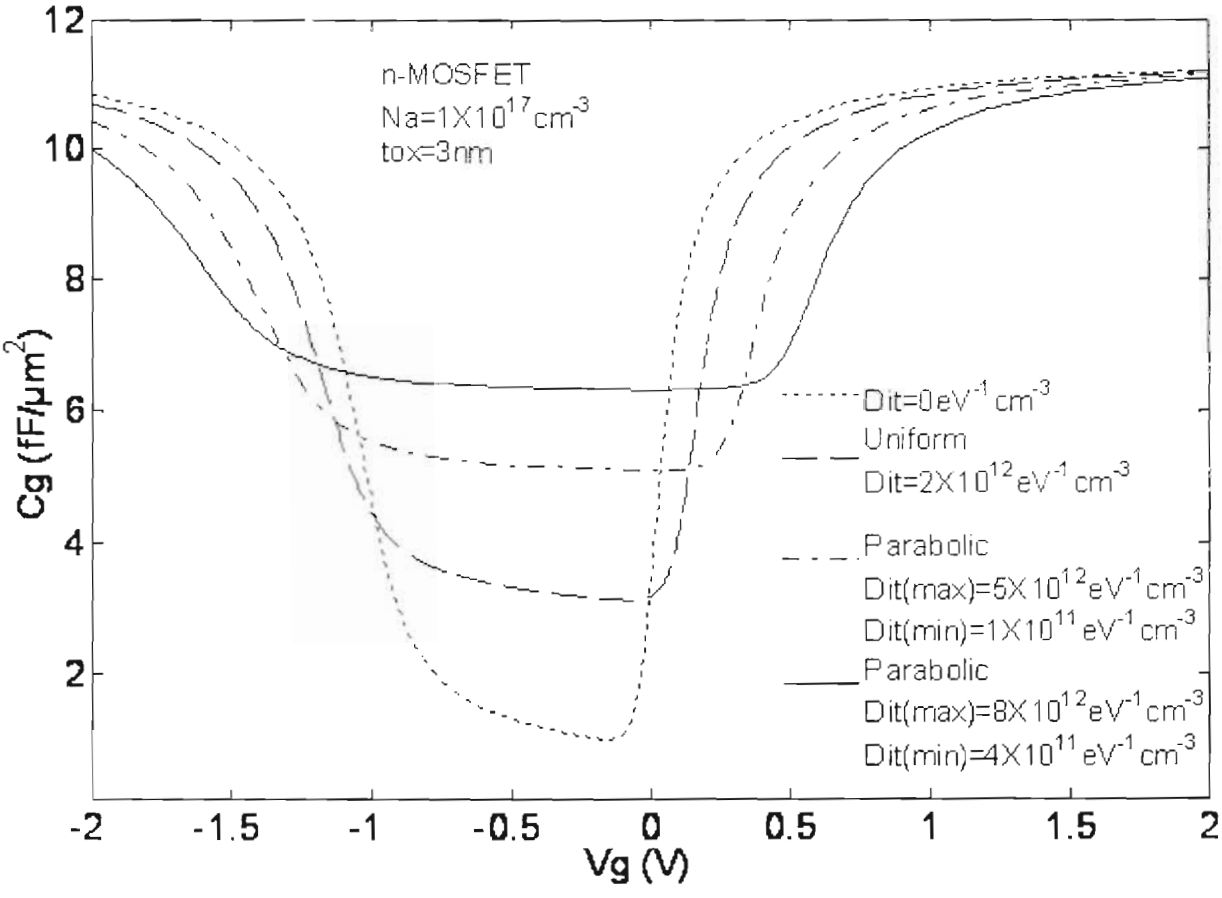


Fig. 4.7: C_g versus V_g curve for SiO_2/Si MOS structure without D_{it}, with uniform D_{it} and parabolic D_{it} profile.

Now we consider Fig. (4.7). The effect of D_{it} on C-V curve is qualitatively similar for higher doping density. We take N_a= 1x 10^{17} cm^{-3} for p type Si considering V_{FB}= -1 V. This figure shows all the changes we have already discussed above.

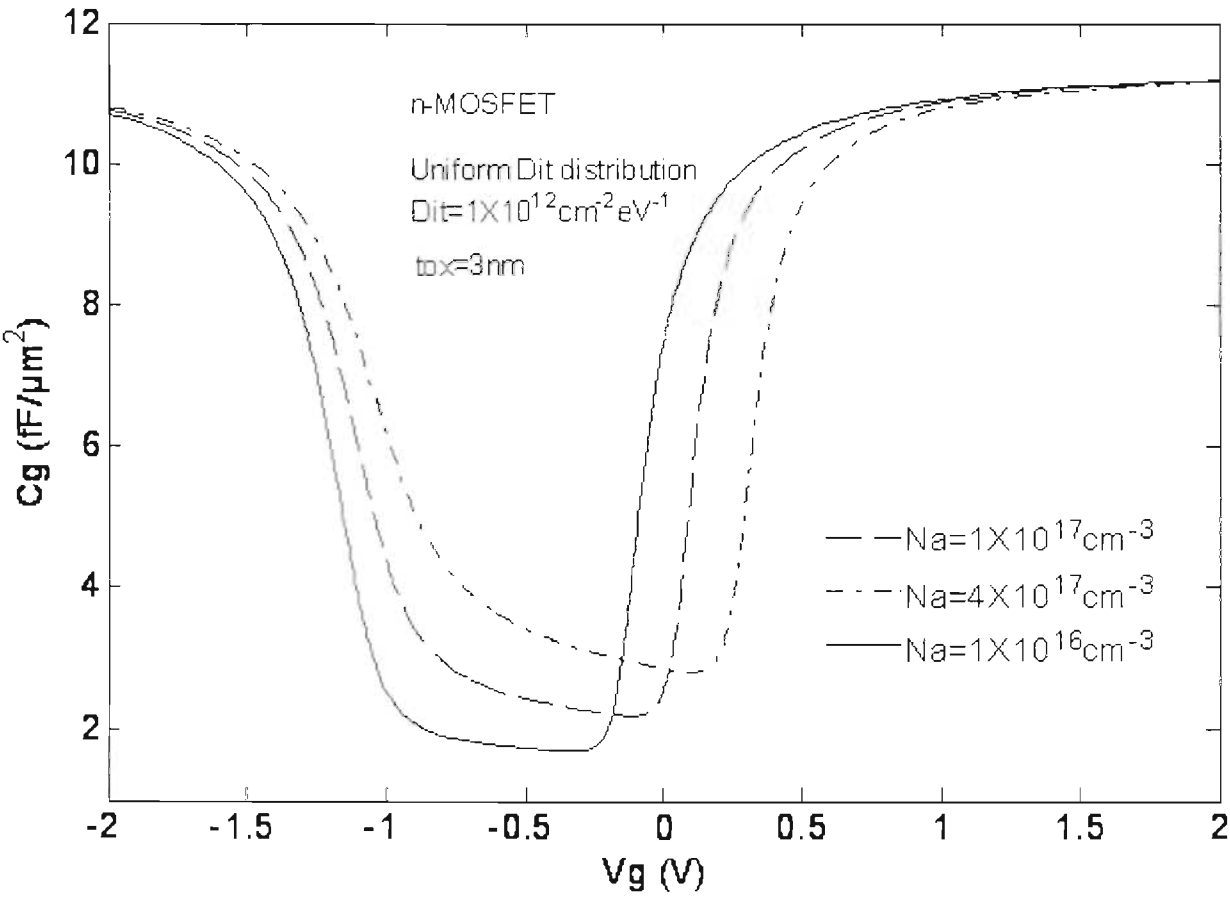


Fig. 4.8: C_g versus V_g curve for SiO_2/Si MOS structure with uniform D_{it} profile of three different doping concentrations.

Now we consider Fig. (4.8) where we have simulated three C-V curves of different doping concentration for a given uniform D_{it} profile. If we observe carefully, the C-V curve shifts to its right and move upward with the increase in doping concentration. The right shift implies an increase of threshold voltage. The minimum value of capacitance is increased with increase in N_a.

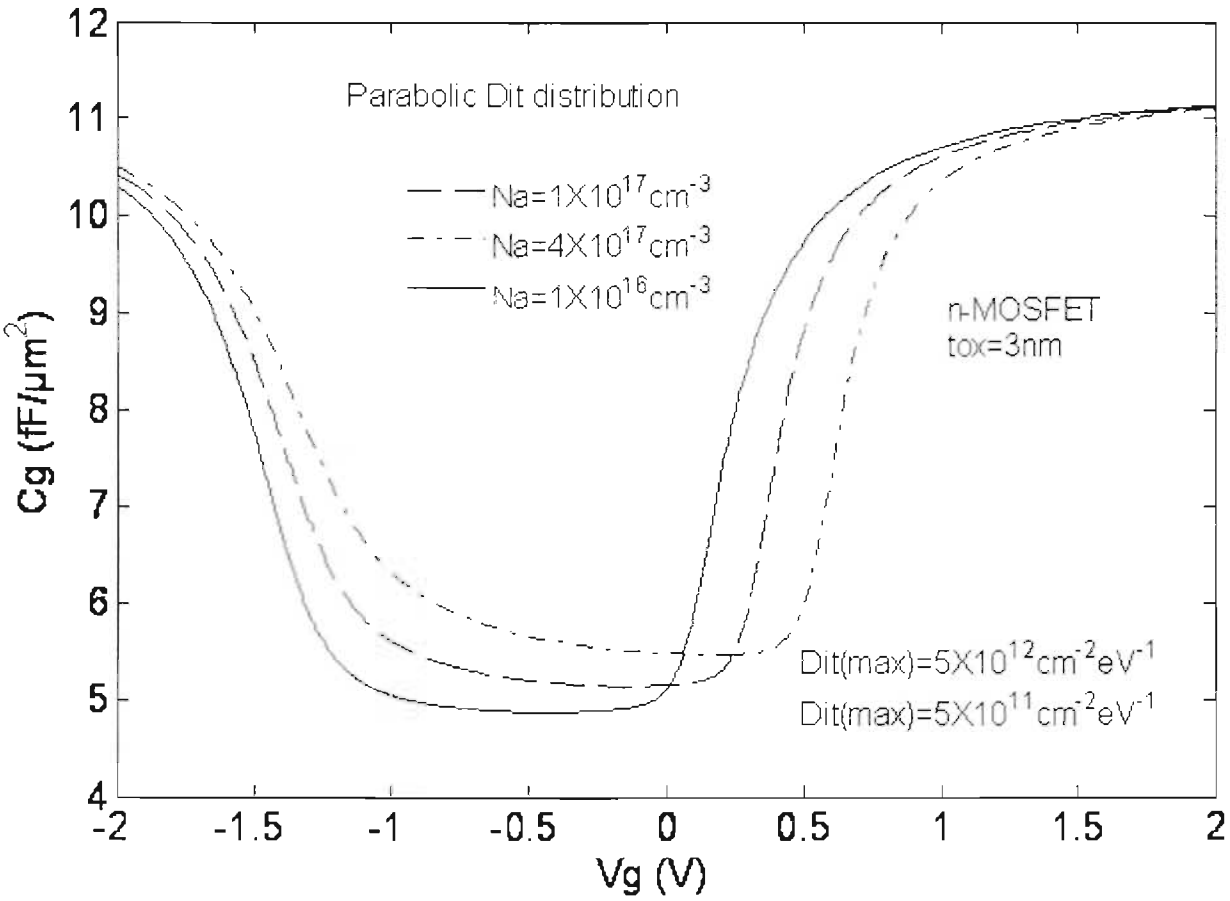


Fig. 4.9: C_g versus V_g curve for SiO_2/Si MOS structure with parabolic D_{it} profile of three different doping concentrations.

Now we consider Fig. (4.9) where we have simulated three C-V curves of different doping concentration taking a parabolic D_{it} profile. Again increasing N_a increases the threshold voltage but for parabolic D_{it}, minimum capacitance increases more slowly with increasing N_a.

Chapter 5

Conclusion

5.1 Summary

A simple model is developed to simulate gate C-V curves with interface trap charge density. It is based on semi-classical theory. Uniform and non-uniform D_{it} are used with different substrate doping densities. Quantum-mechanical (QM) effects are neglected in this study. Although QM models are more accuarate, they are computationally much more involved. Therefore, the proposed model can be useful for a quick study of C-V characteristics including effects of D_{it}.

We have shown that interface trap charges affect every region of C-V characteristics. After including the interface trap charges to calculate C_g, we found that the gate capacitence in accumulation and invertion decreases and in the depletion region the gate capacitence increases. The minimum value of C_g increases.

5.2 Future Works

Our proposed model is based on semi-classical analysis distribution. Many Quantum-mechanical (QM) effects are ignored here.Qm effects may be included in the model. The most accurate way to include QM effects is through the self-consistent solution of Schorodinger's and Poisson's equation. In our model we consider low frequency C-V characteristics. The ac small signal is used to measure the value of the capacitance at the various dc gate biases. Different curves can be obtained for a given device depending on the frequency of the ac signal. Further study on our proposed model can be done in cooperating the effect of the frequency of the ac signal. Our proposed model is valid for up to 2nm gate oxide and thicker gate oxide and here we are not considering gate leakage current. For thinner gate oxide, the gate leakage current is significant. So, further study of gate capacitance can be done considering the effect of gate leakage current.

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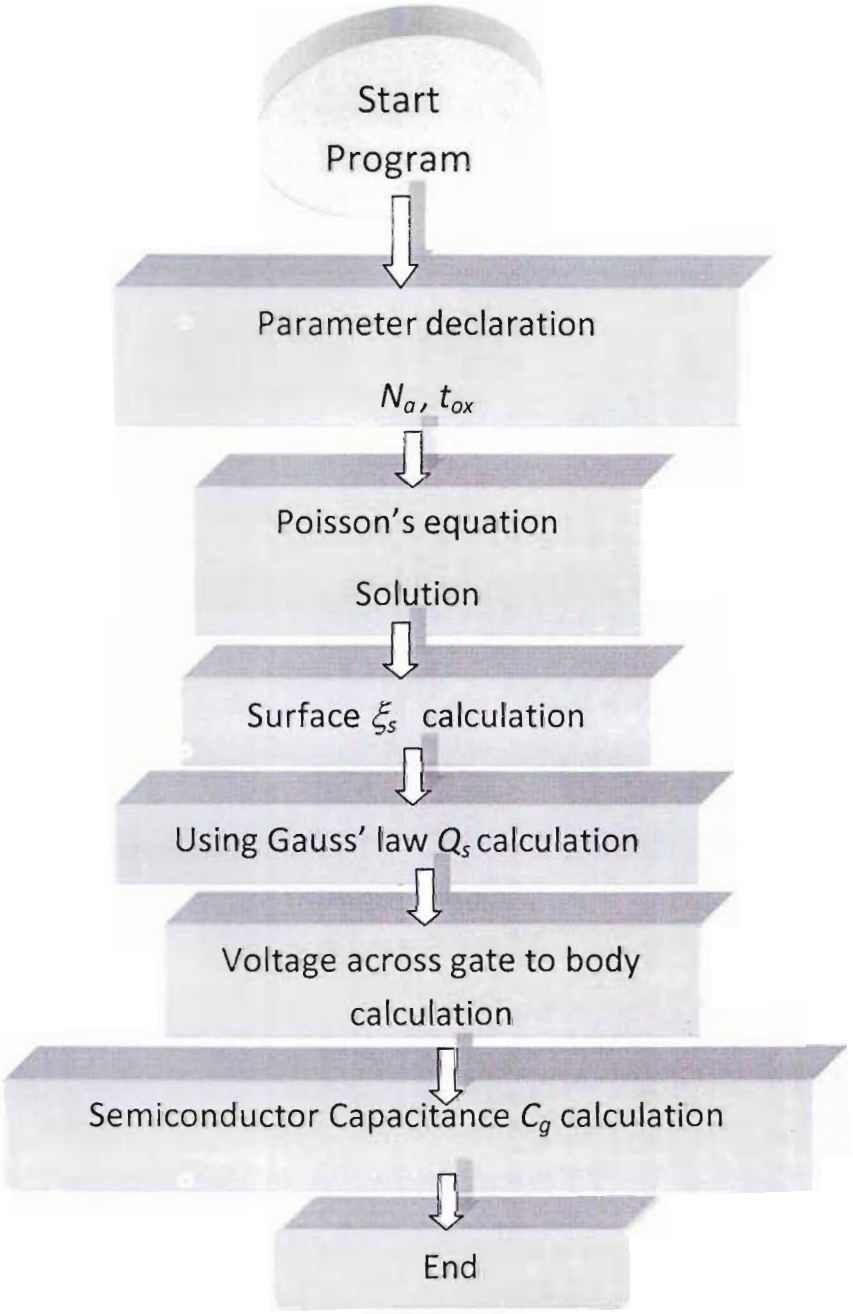
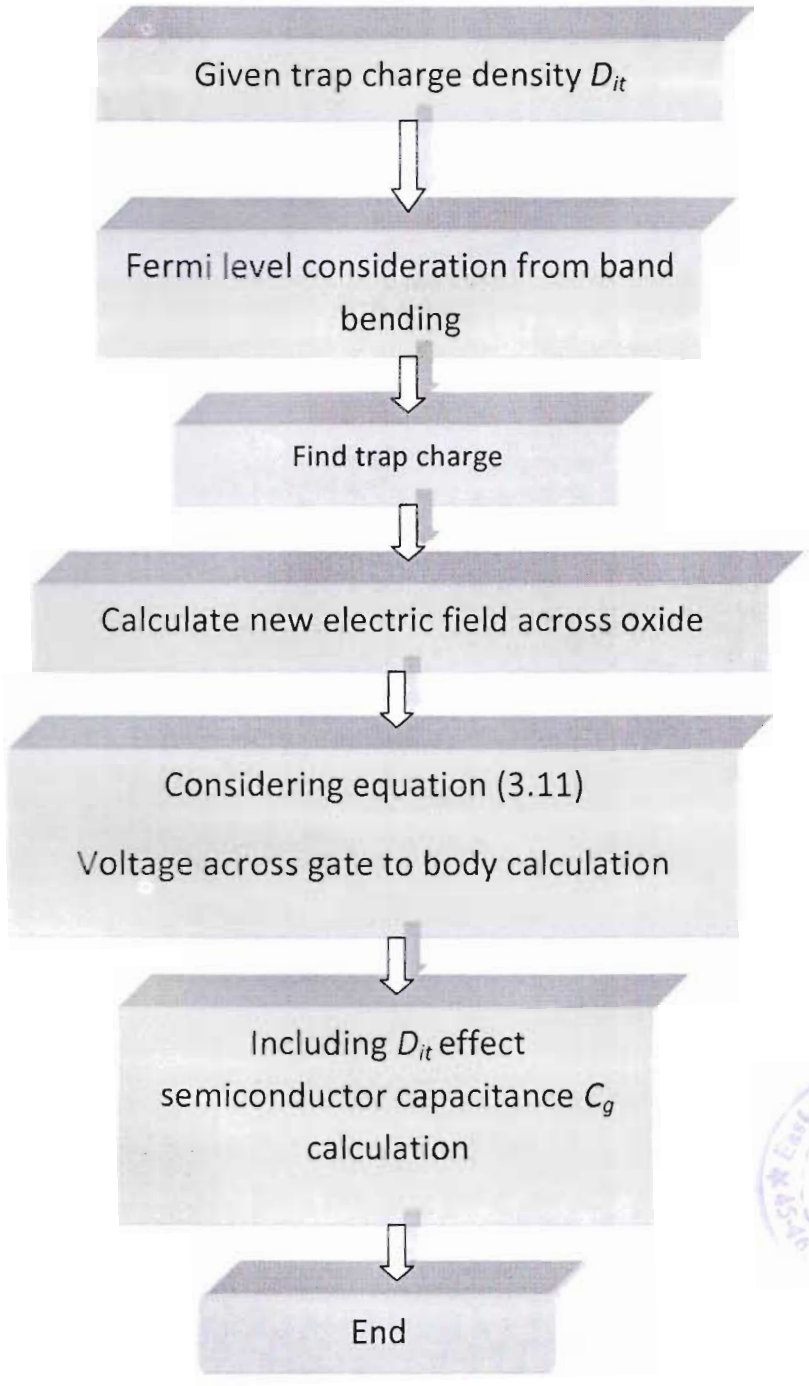
ppendix A No D_{it} effects



cluding D_{it} effects



e A.1: Flow Chart for calculating semiconductor capacitance including no D_{it} effects niform/non-uniform D_{it} effects.