PERFORMANCE COMPARISON BETWEEN INAS ON INSULATOR AND SILICON ON INSULATOR MOSFETS USING A COMPACT MODEL

By

M. A. Al-Mamun,
Shaimum Shahriar, and
Manan Chowdhury

Submitted to the

Department of Electrical and Electronic Engineering
Faculty of Sciences and Engineering
East West University

In partial fulfillment of the requirements for the degree of
Bachelor of Science in Electrical and Electronic Engineering
(B.Sc. in EEE)

Fall, 2011

Approved By

Alam 23/1/2012

Thesis Advisor

Dr. Khairul Alam

23.01.2012

Chairperson

Dr. Anisul Haque

Abstract

Silicon-on-insulator (SOI) MOSFET is one of the modern state of the art transistor in which a semiconductor layer like silicon is formed above an insulator layer on a semiconductor substrate. In SOI MOSFET, there is much more advantages over bulk silicon MOSFET such as high speed operation, low power consumption, small short channel effects. Over the past several years, the inherent scaling limitations of silicon (Si) electron devices have fuelled the exploration of alternative semiconductors, with high carrier mobility, to further enhance device performance. In particular, compound semiconductors heterogeneously integrated on Si substrates have been actively studied: such devices combine the high mobility of III–V semiconductors and the well established, low-cost processing of Si technology. This integration, however, presents significant challenges. Conventionally, heteroepitaxial growth of complex multilayers on Si has been explored but besides complexity, high defect densities and junction leakage currents present limitations in this approach. Motivated by this challenge, we use a three surface potentials (gate oxide-silicon film interface, silicon-film-buried oxide interface and buried oxide-substrate interface) based compact model to study a fully depleted SOI and XOI MOSFETs. We have simulated the surface potentials, surface charge density, gate capacitance, drain current, transconductance and unity gain frequency of SOI and XOI MOSFETs. The different output characteristics show a better performance for InAs. We have got high drain current, transconductance and unity gain frequency of XOI MOSFET. On the other hand, we got very low (negative) threshold voltage for XOI MOSFET. So, by using XOI MOSFET, we can get high speed operation and amplification, low power consumption than SOI MOSFET as well as bulk silicon MOSFET.

Acknowledgements

First of all, we are grateful to the Almighty Allah for giving us this opportunity to complete the research. Then we are grateful to our parents for their incomparable support.

We owe our deepest gratitude to our thesis advisor, Dr. Khairul Alam, Associate Professor, Department of Electrical and Electronic Engineering, East West University, whose constant guidance, supervision, constructive suggestions and constant support giving us direction and providing resources from the initial to the final level of thesis to develop an understanding of the subject.

We thank our chairperson Dr. Anisul Haque and all the faculty members of Department of Electrical and Electronic Engineering, East West University for developing a concept about the research topic in their class lecture for doing the thesis which was so helpful.

We are heartily thankful to Mr. Mahumudur Rahman Siddiqui, Former Research Lecturer, Department of Electrical and Electronic Engineering, East West University, who supported us regarding the basic aspects of this thesis.

We also thank to all of our friends and well wishers for their moral support and helpful discussion during this thesis.

Authorization page

We hereby declare that we are the sole authors of this thesis. We authorize East West University to lend this thesis to other institutions or individuals for the purpose of scholarly research.

Mamun	Shaimum Shahriar	
M. A. Al-Mamun	Shaimum Shahriar	Manan Chowdhury

We further authorize East West University to reproduce this thesis by photocopy or other means, in total or in part, at the request of other institutions or individuals for the purpose of scholarly research.

Mamun	Shaimum Shahriar	
M. A. Al-Mamun	Shaimum Shahriar	Manan Chowdhury

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. INTRODUCTION

In electronics, a SOI MOSFET is a Silicon on Insulator (SOI) structure in which a semiconductor layer, like silicon, germanium, is formed above an insulator layer which may be a buried oxide (BOX) layer formed on a semiconductor substrate as shown in Figure 1-1. SOI devices are laterally isolated from each other by an insulator film and vertically isolated from the substrate by the BOX, which makes the isolation ideal. As a result, SOI devices can be packed closer together than the bulk ones. In addition, the n+ and p+ diffusion regions at the output of a CMOS inverter can be connected directly to each other, which make the area of a device smaller than that of a bulk one [1].

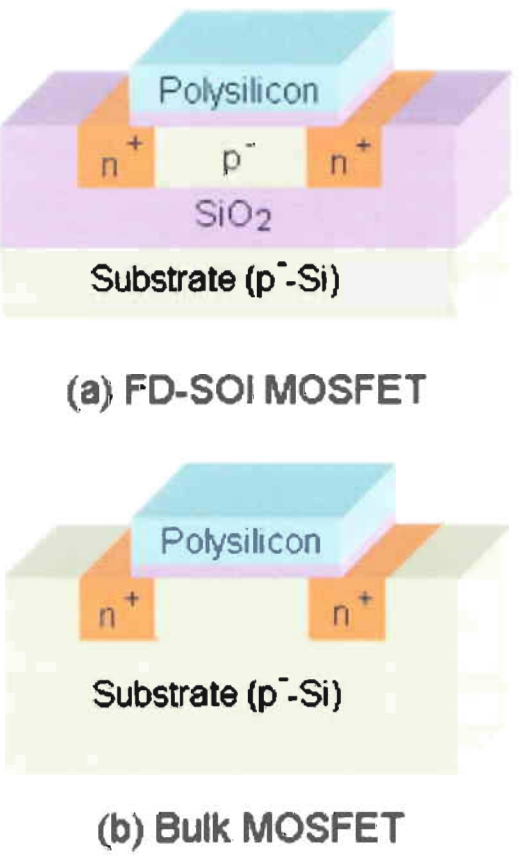

Figure 1-1: Structure of a FD-SOI MOSFET and a bulk MOSFET [1]

The SOI technology is introduced to overcome the limits of bulk or conventional Si MOSFETs. Among the problems are that the carrier mobility is decreasing due to impurity scattering, the gate tunneling current is increasing as the gate insulator becomes thinner, and the p-n junction leakage is increasing as the junction becomes shallower. These trends make the conventional scaling less and less feasible. As a result, the operating voltage is set higher than the expected value of a scaled-down device to achieve the desired speed performance and therefore the power dissipation goes high [2].

In a bulk Si CMOS technology, scaling down the channel length results in a roll-off of the threshold voltage, which is called short channel effect. It is due to the loss of control by the gate to part of the depletion zone below it. In order to minimize the short channel effect, one should increase the doping level in channel region. This increases drain capacitance and results in an increase in inverse sub threshold slope. In a partially depleted SOI structure, the short channel effects are not as serious as in bulk Si CMOS. Therefore, it is possible to optimize channel doping profile to achieve better inverse sub threshold slope with minimum short channel effects. In a thin film SOI device, the channel region is fully depleted. This results in an inverse sub threshold slope in FD SOI MOSFET close to the ideal value of 60 mV/decade. The lower inverse sub threshold slope is highly desirable for low-power low-voltage applications because it allows the use of devices with a smaller value of threshold voltage without an increase in leakage current. This reduces the static power consumption significantly [3].

Silicon-on-insulator technology features a low capacitance, which enables high-speed operation. That is, the supply voltage can be lowered to cut power consumption while adequate speed is provided. In SOI devices, the capacitance between the drain (source) and the substrate is negligibly small because of the dielectric constant of SiO_2, which is lower than that of Si, and the thickness of the BOX. This helps improve the switching speed of CMOS devices, as can be seen in the relationship between power consumption and access time for a 4-Mb SRAM shown in Figure 1-2. For a given access speed, SOI devices consume only one-half to one-third the power of bulk Si devices; and for a given power consumption, they are 20% to 25% faster. This amount of improvement is typical for SOI CMOS [4].

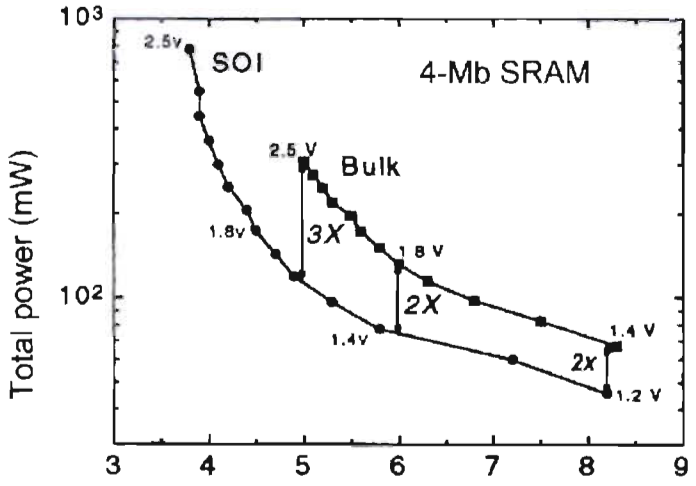

Figure 1-2: Speed and power consumption of bulk-Si and SOI MOSFETs [4]

SOI CMOS offers a higher integration density than bulk CMOS. This high density results mainly from the absence of wells in SOI technology. SOI CMOS devices can be isolated by reach through oxidation, while bulk devices normally use junction isolation. SOI wafers can be processed in standard bulk silicon processing lines. As the feature size scaled down in modern IC technology, the source drain junction depth needs to be reduced to suppress short channel effects. In bulk silicon devices, such reduction may bring an unwanted interaction between the silicon and the metal such as metal punching through the junction. If the device is built on an SOI wafer, the source drain junction sits directly on dielectric layer (BOX) and no leakage occurs even the metal punches through the junction [3].

In conventional bulk CMOS technology, special care must be taken to prevent latch up. Latch up occurs because of the parasitic PNPN structure inherent in the CMOS structure. The latch up path in bulk CMOS can be symbolized by two bipolar transistors formed by the substrate, the well and the source and drain junctions. Latch up can be triggered by different mechanisms such as node voltage overshoot, junction avalanching and photocurrents. A necessary condition for latch up occurrence is that the current gain of the loop formed by the two bipolar transistors is larger than unity. In an SOI CMOS inverter, the silicon film containing the active devices is thin enough for the junctions to reach through to the buried insulator. A latch up path is ruled out because there is no current path to the substrate [3].

However, the advantages of SOI technology are not limited to the areas of speed and power; they also include good radiation hardness, the ability to withstand high temperatures, and the ability to handle high voltages. This technology also enables the fabrication of micro-electro-mechanical systems (MEMS) for control systems. Furthermore, it allows flexible device design; for example, the properties of the substrate can be set independently of those of the device layer because an insulator separates devices from the substrate. The fully-depleted (FD) SOI MOSFET is a special type of SOI MOSFET. In addition to high speed and low power, it exhibits steep sub threshold characteristics, negligible floating-body effects, and small short-channel effects [2].

1.1. Development of SOI MOSFET

The idea of building MOSFET on an insulator goes back to the 1960s, and first implemented in the thin-film transistor (TFT). The first SOI transistors, dates back to 1964, were partially depleted devices fabricated on silicon-on-sapphire (SOS) substrates. SOS devices were expected to provide high-speed performance because of their low capacitance, and they were actually used to make high-speed logic LSIs until the early 90s. However, SOS eventually gave way to bulk-Si technology in the high-speed area, because of some serious drawbacks: The high dislocation density arising from the lattice mismatch at the sapphire/Si interface caused a non-negligible leakage current in MOSFET. The aluminum in the sapphire substrate tended to migrate into the epitaxial film, complicating the fabrication process. The residual compressive strain due to the large difference between the coefficients of thermal expansion of sapphire and Si degraded the electron mobility. Finally, floating-body effects produced abnormal behavior that negatively impacted circuit operation [2].

The first industrial implementation of SOI was announced by IBM in August 1998 and in 1999, IBM launched the first fully functional SOI mainstream microprocessor. The IBM specifications predict a 25-35% improvement over similar bulk CMOS technology, which is equivalent to about two years of progress in bulk CMOS design and fabrication. Besides the fast speed, other benefits of the new SOI chip are reduced power consumption (up to 3 times) and a small soft error rate [5].

1.2. Fully Depleted versus Partially Depleted SOI MOSFET

With silicon-on-insulator (SOI) technology, MOSFETs are formed in a thin top Si layer (SOI layer) separated from the Si substrate by an insulating film. This structural feature provides SOI devices with several advantages for high-speed, low-power operation. SOI devices are divided into two types, depending on the operating mode: fully-depleted (FD) and partially-depleted (PD). The difference mainly derives from the thickness of the SOI layer, with the layer generally being thinner for FD-SOI devices. In PD-SOI devices, there is an undepleted neutral region at the bottom of the SOI layer; but in FD-SOI devices, the entire body region is fully depleted. This provides FD-SOI devices with additional advantages, such as a low threshold voltage, a small leakage current, and smaller floating-body effects. Because of these features, FD-SOI devices exhibit better performance at low supply voltages; and lowering the supply voltage is one of the most effective ways to reduce power consumption [1].

Fully Depleted SOI MOSFET

In an NMOS transistor, applying a positive voltage to the gate depletes the body of P-type carriers and induces an N-type inversion channel on the surface of the body. If the insulated layer of silicon is made very thin, the layer fills the full depth of the body [1].

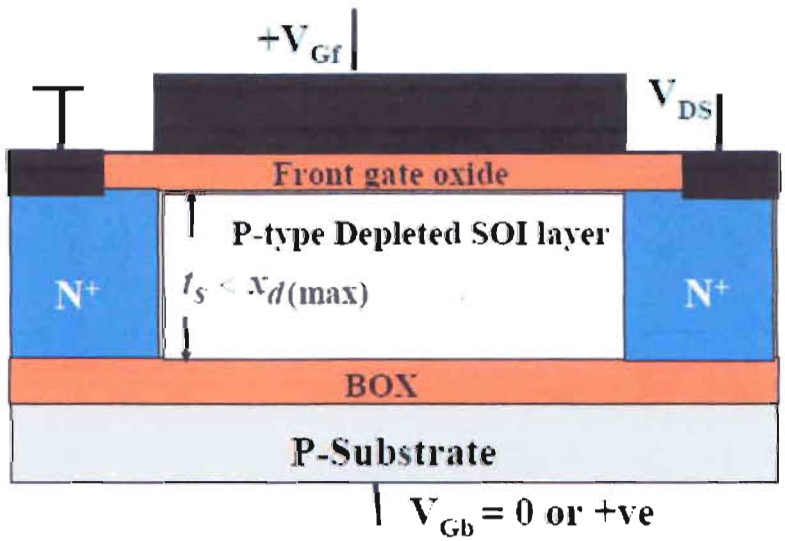

Figure 1-3: FD SOI with totally depleted region [1]

A technology designed to operate this way is called a "fully depleted" SOI technology. The thin body avoids a floating voltage. In 45nm and below CMOS, the V_{th} (threshold voltage) can be tuned by a midgap metal gate leaving the fully-depleted body undoped. Higher channel mobility and hence higher performance are achieved, as well as lower variability from one device to another. Fully Depleted SOI enables a CMOS LP technology with un-doped body. It gives the best performance - low leakage couple, a perfect choice for Low Power Applications. Figure 1-3 shows a fully depleted SOI MOSFET structure [1].

Partially Depleted SOI MOSFET

On the other hand, if the insulated layer of silicon is made thicker, the inversion region does not extend the full depth of the body. A technology designed to operate this way is called a "partially depleted" SOI technology. The undepleted portion of the body is not connected to anything. The exact voltage depends on the history of source, gate, and drain voltages leading up to the current time (the "history effect"). However, the voltage can be expected to fall within a known range [1].

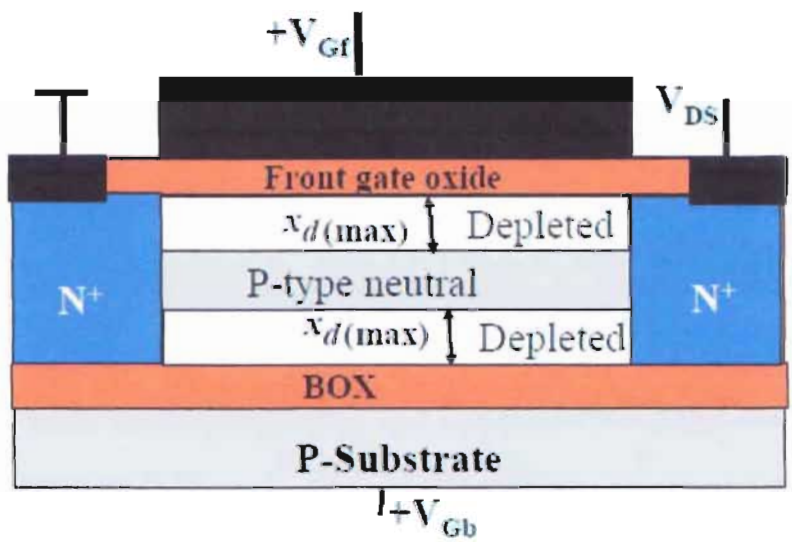

Figure 1-4: PD SOI MOSFET with partially depleted region [1]

The body voltage affects the conduction of the channel and therefore the switching speed and parasitic capacitance of the circuit. In an NMOS transistor, a lower initial body voltage results in a

thinner inversion layer, lower conductivity, and slower switching. Conversely, a higher initial body voltage results in faster switching. In a PMOS transistor, the opposite is true; a lower initial body voltage results in faster switching. Charging of the transistor body (floating body) leads to a change in the threshold voltage, if this is properly taken into account in the IC conception then the result is a faster switching, thus higher performance at same V_{dd}. Figure 1-4 shows a partially depleted SOI MOSFET structure [1].

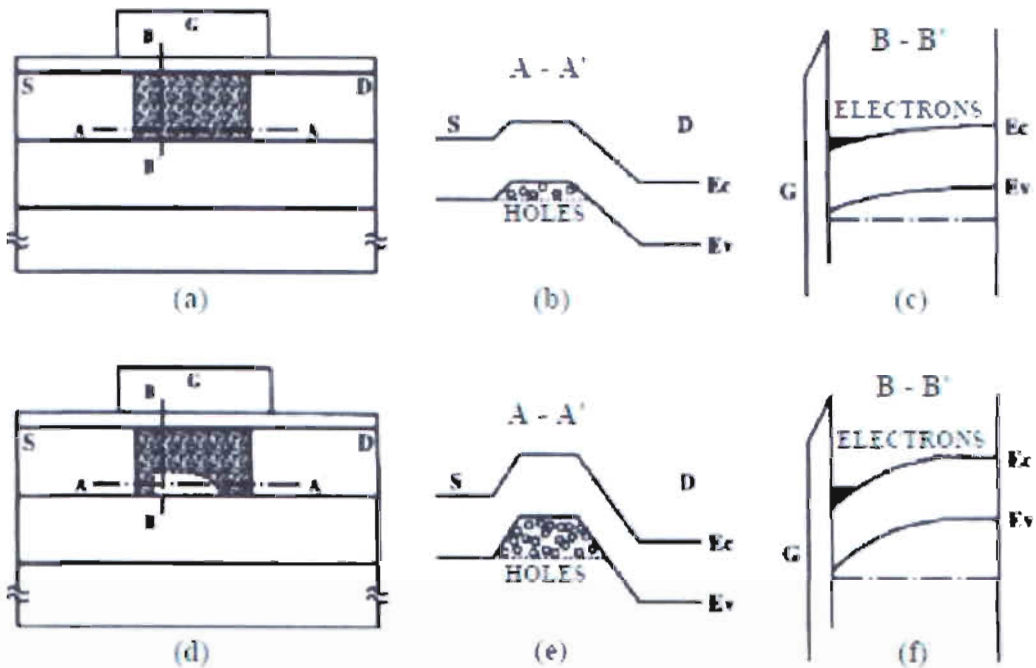

Figure 1-5: FD-SOI and PD-SOI MOSFETs. (a) Cross section of an FD-SOI device, (b) the energy band diagram along the line A-A′, and (c) the energy band diagram along the line B-B′. (d-f) show the corresponding figures for a PD-SOI device [1]

The difference between fully-depleted (FD) and partially-depleted (PD) SOI MOSFETs is described below with reference to Figure 1-5, taking an nMOSFET as an example. In the figure, (a) shows the cross-sectional structure of an FD-SOI MOSFET; (b) is energy band diagram along the line A–A′ in (a), which runs through the source, body, and drain near the bottom of the body region; and (c) is an energy band diagram showing how the energy bands change along the line B–B′ in (a), which runs from the gate oxide film down into the body region near the source end. The corresponding figures for a PD-SOI MOSFET are shown in Figure 1-5(d-f). In a FD-SOI device, the entire body region is depleted in both the 'on' and 'off' states, as shown in Figure 1-5(a). This results

from the fact that a FD-SOI device generally has a thinner body region than a PD-SOI device. For example, the body region is about 100–200 nm thick in a PD-SOI device, but at most about 50 nm thick in a FD-SOI device [1].

In contrast to a FD-SOI device, a PD-SOI device has an undepleted neutral region at the bottom of the body region, as shown in (d). This difference results in a different potential distribution inside the body region. In a FD-SOI device, the entire body region has a potential gradient in the depth direction, as shown in (c); and the gate field extends right into the BOX. In a PD-SOI device, the influence of the gate field stops inside the body region, as shown in (f); and there is a neutral region with no potential gradient at the bottom of the body region. Accordingly, the potential difference between the top and bottom of the body region is larger in a PD-SOI device; and the potential barrier to holes between the source and body near the bottom of the body region is higher [1].

This difference in the barrier height for holes leads to a difference in the number of holes that accumulate in the body region. Holes are generated by impact ionization near the drain. During the operation of an nMOSFET, when channel electrons pass through the high-electrical-field region near the drain, they gain energy from the field and jump to higher energy levels. The high-energy electrons collide with valence electrons and generate more electrons and holes (impact ionization). The electrons flow into the drain, and the holes flow toward the source via the bottom of the body region. When this happens, more holes accumulate at the bottom of the body region in a PD-SOI than in a FD-SOI device because a PD-SOI device has a higher potential barrier. This leads to a large difference between the floating-body effects of the two types of devices, such as the kink in the drain current-voltage characteristics and the stability of the dynamic characteristics [1].

1.3. Short Channel Effects

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise [6].

The short-channel effects are attributed to two physical phenomena:

a) The limitation imposed on electron drift characteristics in the channel,

b) The modification of the threshold voltage due to the shortening channel length.

In particular five different short-channel effects can be distinguished:

a) Drain-induced barrier lowering and punchthrough

b) Surface scattering

c) Velocity saturation

d) Impact ionization

e) Hot electrons

Drain-induced barrier lowering and punchthrough

The expressions for the drain and source junction widths are:

$$x_{dD} = \sqrt{\left(\frac{2\varepsilon_{Si}}{qN_A}\right)(V_{DS} + \varphi_{Si} + V_{SB})}$$

and

$$x_{dS} = \sqrt{\left(\frac{2\varepsilon_{Si}}{qN_A}\right)(\varphi_{Si} + V_{DB})}$$

where V_{SB} and V_{DB} are source-to-body and drain-to-body voltages [7].

When the depletion regions surrounding the drain extends to the source, so that the two depletion layer merge (i.e., when $x_{dS} + x_{dD} = L$), punchtrough occurs. Punchthrough can be minimized with thinner oxides, larger substrate doping, shallower junctions, and obviously with longer channels. The current flow in the channel depends on creating and sustaining an inversion

layer on the surface. If the gate bias voltage is not sufficient to invert the surface ($V_{GS} < V_{th}$), the carriers (electrons) in the channel face a potential barrier that blocks the flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage V_{GS} and the drain-to-source voltage V_{DS}. If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under this conditions ($V_{GS} < V_{th}$) is called the sub-threshold current [7].

Surface scattering

As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component ε_y increases, and the surface mobility becomes field-dependent. Since the carrier transport in a MOSFET is confined within the narrow inversion layer, and the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by ε_x) causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of ε_y, is about half as much as that of the bulk mobility [7].

Velocity Saturation

The performance of short-channel devices is also affected by velocity saturation, which reduces the transconductance in the saturation mode. At low ε_y, the electron drift velocity (v_{de}) in the channel varies linearly with the electric field intensity. However, as ε_y increases above 10^4 V/cm, the drift velocity tends to increase more slowly, and approaches a saturation value of $v_{de(sat)}$ = 10^7 cm/s around ε_y =10^5 V/cm at 300 K. The drain current is limited by velocity saturation instead

of pinchoff. This occurs in short channel devices when the dimensions are scaled without lowering the bias voltages [8].

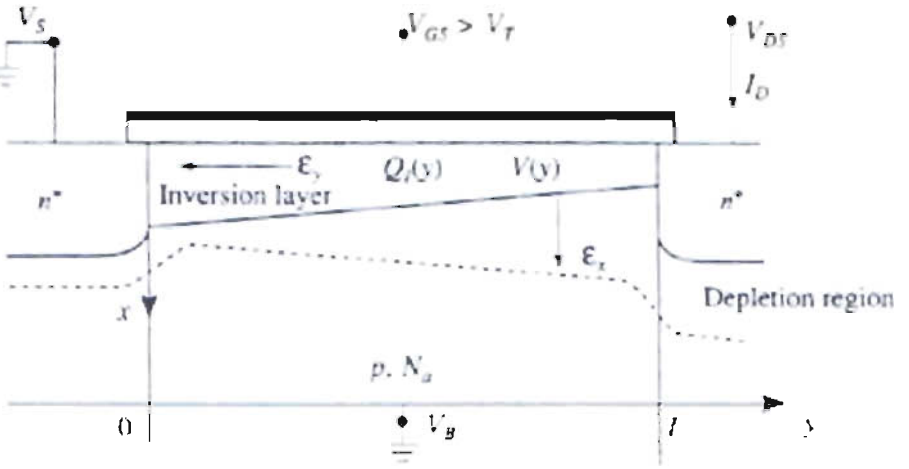

Figure 1-6: Surface charge distribution in a bulk MOSFET [8]

Using $v_{de(sat)}$, the maximum gain possible for a MOSFET can be defined as [8]

$$g_m = WC_{ox}v_{de(sat)}$$

Impact ionization

Another undesirable short-channel effect, especially in NMOS, occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole (e-h) pairs by impact ionization, that is, by impacting on silicon atoms and ionizing them. It happens as follow: normally, most of the electrons are attracted by the drain, while the holes enter the substrate to form part of the parasitic substrate current [7]. Moreover, the region between the source and the drain can act like the base of an NPN transistor, with the source playing the role of the emitter and the drain that of the collector. If the aforementioned holes are collected by the source, and the corresponding hole current creates a voltage drop in the substrate material of the order of 0.6V, the normally reversed-biased substrate-source PN junction will conduct appreciably. Then electrons can

be injected from the source to the substrate, similar to the injection of electrons from the emitter to the base. They can gain enough energy as they travel toward the drain to create new e-h pairs. The situation can worsen if some electrons generated due to high fields escape the drain field to travel into the substrate, thereby affecting other devices on a chip [8].

Hot electrons

Another problem, related to high electric fields, is caused by so-called hot electrons. These high energy electrons can enter the oxide, where they can be trapped, and giving rise to oxide charging that can accumulate with time and degrade the device performance by increasing V_{th} (threshold voltage) and affect adversely the gate's control on the drain current [8].

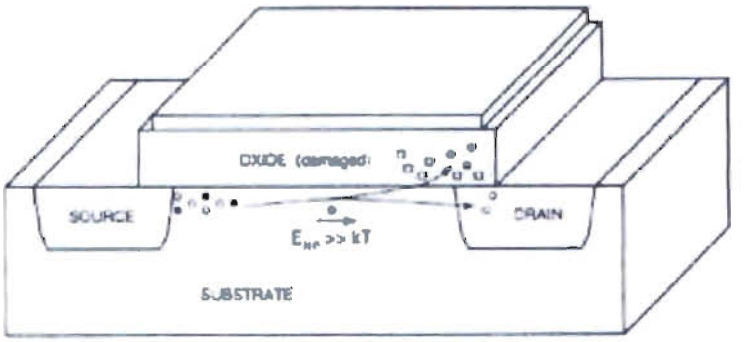

Figure 1-7: Hot electrons in a bulk MOSFET [8]

1.4. Self Heating Effects

Self heating is due to the thermal isolation of transistors from the substrate by the buried insulator. As a result, removal of excess heat generated within the SOI devices is less efficient than in bulk devices, which may result in a substantial increase in device operating temperature. Due to thermal isolation of substrate by the buried insulator in an SOI transistor, removal of excess heat

generated by the Joule effect within the device is less efficient than in bulk, which leads to substantial elevation of device temperature. The excess heat mainly diffuses vertically through the buried oxide and laterally through the silicon island into the contacts and metallization. Due to the relatively low thermal conductivity of the buried oxide, the device heats up to 50° C to 150° C. This increase in device temperature leads to a reduction in mobility and current drive, thus degrading the device performance over a period of time [4].

1.5. Objective of our work

The main objective of our work is performance comparison between InAs-on-Insulator and Silicon-on-Insulator MOSFETs using a compact model. First of all, we follow a model as discussed in Ref. [9] which uses three surface potentials. However, before proceed to our objective, we want to verify our model with the results of Ref. [9]. After verifying the model, we want to change the channel material to InAs by replacing Si and then to compare the performance. For fair comparison the device dimensions, doping densities will be assumed same. Then after calculating surface potential, using this we want to compare the C-V characteristics and the drain current. From the I_D-V_{GS} curve, we can calculate the threshold voltage, on and off current ratio of the MOSFET. Then we also want to observe the difference between transconductance and unity gain frequency of InAs-on-Insulator and Silicon-on-Insulator MOSFET.

2. MODEL

2.1. Ideal Surface Potential Model

Surface potential based MOSFET models provide consistent and accurate expressions for terminal currents and charges valid in all regions of operations. These models have emerged as a better alternative to the threshold voltage based models as they are suitable for simulating circuits with low power supply voltages and also allow physical modeling of the subthreshold region, which were the main drawbacks of the threshold-voltage-based models [10]. Many models based on surface potential approach have been developed for bulk MOSFETs and implemented in different circuit simulators. The same modeling approach has been extended to partially depleted silicon-on-insulator (SOI) (PDSOI) MOSFET with a special consideration to effects, specific to PDSOI MOSFET, such as floating body and self-heating effects. However, modeling of fully depleted SOI (FDSOI) MOSFET is quite different due to appearance of depletion charge in the substrate region. To obtain a closed-form analytical approximation for potentials at the three surfaces of the FDSOI MOSFET, namely front oxide–silicon film surface φ_s, buried oxide–silicon film interface φ_{sb}, and buried oxide–substrate interface φ_{sbulk}. For this purpose, three different equations are obtained by solving the 1-D Poisson equation in vertical direction and applying the boundary conditions at different surfaces [9].

The 1-D Poisson equation of an FD-SOI MOSFET, shown in Figure 2-1, can be written as

$$\frac{\partial^2 \varphi(y)}{\partial y^2} = -\frac{1}{\varepsilon_{Si}}\left(p(y) - n(y) - N_{ch}\right) \quad \text{..... (1)}$$

Where $\varphi(y)$ is the potential, ε_{Si} is the dielectric constant of silicon, $p(y)$ and $n(y)$ are the hole and electron concentrations, respectively and N_{ch} is the doping in the silicon layer [9].

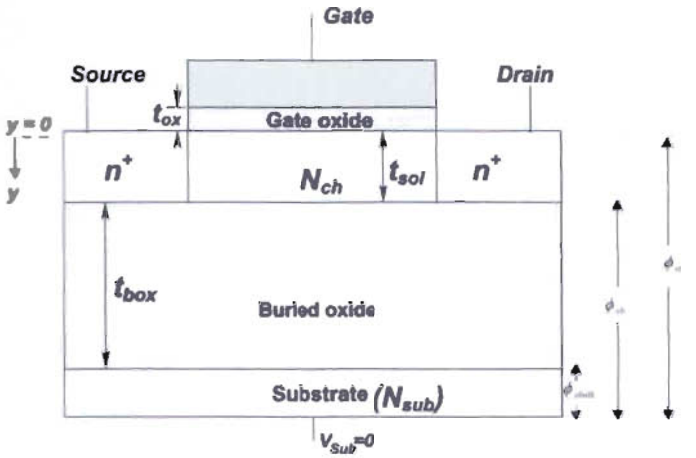

Figure 2-1: Cross-sectional view of the FD SOI MOSFET [9]

Equation (1) can be further expressed as

$$\frac{\partial^2 \varphi(y)}{\partial y^2} = -\frac{qN_{ch}}{\varepsilon_{Si}} \left\{ \left[\exp\left(-\frac{\varphi(y)}{\varphi_t} \right) - 1 \right] - \exp\left(-\frac{2\varphi_F + V_{CB}}{\varphi_t} \right) \left[\exp\left(\frac{\varphi(y)}{\varphi_t} \right) - 1 \right] \right\} \quad \ldots. (2)$$

where φ_F is the Fermi potential, φ_t is the thermal voltage, and V_{CB} is the channel floating body potential, which varies from V_{SB} at source to $V_{SB} + V_{DS}$ at drain [9].

Multiplying both sides of Eq. (2) by $2\frac{\partial \varphi(y)}{\partial y}$ and then integrating from buried oxide–silicon film interface φ_{sb} to front oxide–silicon film surface φ_{sf}, we get

$$\left[\left. \frac{\partial \varphi(y)}{\partial y} \right|_{\varphi(y)=\varphi_{sf}} \right]^2 - \left[\left. \frac{\partial \varphi(y)}{\partial y} \right|_{\varphi(y)=\varphi_{sb}} \right]^2 = -\frac{2qN_{ch}}{\varepsilon_{Si}} \left\{ \begin{array}{l} -\varphi_t \left[\exp\left(-\frac{\varphi_{sf}}{\varphi_t} \right) - \exp\left(-\frac{\varphi_{sb}}{\varphi_t} \right) \right] \\ -\left(\varphi_{sf} - \varphi_{sb} \right) - \exp\left(-\frac{2\varphi_F + V_{CB}}{\varphi_t} \right) \\ \left(\varphi_t \left[\exp\left(\frac{\varphi_{sf}}{\varphi_t} \right) - \exp\left(\frac{\varphi_{sb}}{\varphi_t} \right) \right] - \left(\varphi_{sf} - \varphi_{sb} \right) \right) \end{array} \right\}$$

$\ldots\ldots\ldots\ldots\ldots\ldots$ (3)

The following boundary conditions need to be used in equation (3):

1) Electric flux (displacement) at the front oxide/Si film interface is continuous.

$$-\left.\frac{\partial\varphi(y)}{\partial y}\right|_{\varphi(y)=\varphi_{sf}} = \frac{V_g-\varphi_{sf}}{t_{ox}}\frac{\varepsilon_{ox}}{\varepsilon_{Si}} \quad \text{.....(4)}$$

where ε_{ox} is the dielectric constant of the gate oxide, t_{ox} is the front gate oxide thickness, and $V_g = V_{GS} - V_{FB}$, where V_{GS} is the gate-to-source bias voltage and V_{FB} is the flat-band voltage.

2) Electric flux at the interface of the buried oxide/Si film is continuous.

$$-\left.\frac{\partial\varphi(y)}{\partial y}\right|_{\varphi(y)=\varphi b} = \frac{\varphi_{sb}-\varphi_{sbulk}}{t_{box}}\frac{\varepsilon_{box}}{\varepsilon_{Si}} \quad \text{.....(5)}$$

where ε_{box} is the dielectric constant of the burried oxide, t_{box} is the buried oxide thickness, φ_{sb} is the surface potential at the buried oxide–silicon layer, and φ_{sbulk} is the surface potential at the buried oxide–substrate interface [9].

Substituting the two aforementioned boundary conditions in Eq. (3) we get

$$\left(V_g-\varphi_{sf}\right)^2 - \frac{C_{box}^2}{C_{ox}^2}\left(\varphi_{sbulk}-\varphi_{sb}\right)^2 = -\gamma^2\left\{\begin{array}{l} -\varphi_t\left[\exp\left(-\frac{\varphi_{sf}}{\varphi_t}\right)-\exp\left(-\frac{\varphi_{sb}}{\varphi_t}\right)\right] \\ -\left(\varphi_{sf}-\varphi_{sb}\right)-\exp\left(-\frac{2\varphi_F+V_{CB}}{\varphi_t}\right) \\ \left(\varphi_t\left[\exp\left(\frac{\varphi_{sf}}{\varphi_t}\right)-\exp\left(\frac{\varphi_{sb}}{\varphi_t}\right)\right]-\left(\varphi_{sf}-\varphi_{sb}\right)\right) \end{array}\right\}$$

..... (6)

where $\gamma = \frac{\sqrt{2qN_{ch}\varepsilon_{Si}}}{C_{ox}}$, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ and $C_{box} = \frac{\varepsilon_{box}}{t_{box}}$

Equation (6) has three unknowns namely φ_{sf}, φ_{sb} and φ_{sbulk}. Therefore, two more equations are needed to solve it and they can be obtained by solving the Poisson equation in the silicon film layer and the substrate region [9].

Assuming inversion at the back silicon film surface and the substrate to be absent, the Poisson equations for the substrate and silicon film are given by Eqs. (7) and (8), respectively

$$\frac{\partial^2 \varphi(y)}{\partial y^2} = -\frac{1}{\varepsilon_{Si}}(-qN_{sub}) \quad \text{..... (7)}$$

$$\frac{\partial^2 \varphi(y)}{\partial y^2} = -\frac{1}{\varepsilon_{Si}}(-qN_{ch}) \quad \text{..... (8)}$$

For simplicity, we have ignored the small voltage drop appearing across the front surface inversion charge layer while writing Eq. (8).

Multiplying both sides of Eqs. (7) and (8) by $2\frac{\partial \varphi(y)}{\partial y}$, and then integrating Eq. (7) from the buried oxide-substrate interface $[\varphi(y) = \varphi_{sbulk}]$ to deep neutral substrate region $[\varphi(y) = 0]$ and Eq. (8) from a point y distance below the front oxide-silicon film interface $[\varphi(y)]$ to the buried oxide-silicon film interface $[\varphi(y) = \varphi_{sb}]$, we arrive at the following equations, respectively:

$$\left[\left.\frac{\partial \varphi(y)}{\partial y}\right|_{\varphi(y)=\varphi(y)}\right]^2 - \left[\left.\frac{\partial \varphi(y)}{\partial y}\right|_{\varphi(y)=\varphi_{sb}}\right]^2 = \frac{2qN_{ch}}{\varepsilon_{Si}}(\varphi(y) - \varphi_{sb}) \quad \text{..... (9)}$$

$$\left[\left.\frac{\partial \varphi(y)}{\partial y}\right|_{\varphi(y)=\varphi_{sbulk}}\right]^2 = \frac{2qN_{sub}}{\varepsilon_{Si}}(\varphi_{sbulk}) \quad \text{..... (10)}$$

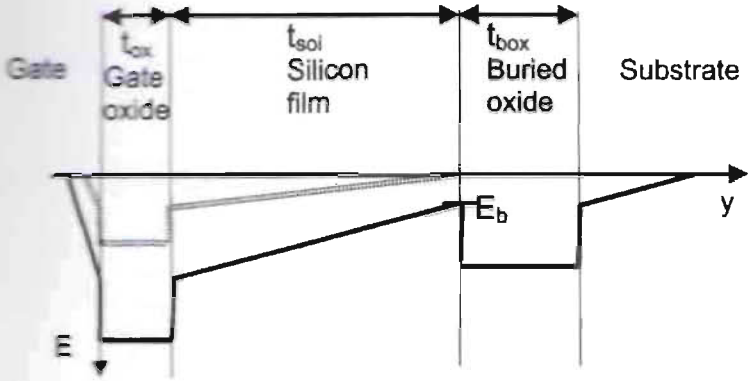

Figure 2-2: Electric field profile from the Si/SiO_2 interface of the front gate oxide toward the substrate. The solid lines indicate the electric field distribution for a given gate voltage. The dashed lines show the electric field when the silicon film is just depleted [9]

By noting the identity $\left.\frac{\partial\varphi(y)}{\partial y}\right|_{\varphi(y)=\varphi_{sbulk}} = \left.\frac{\partial\varphi(y)}{\partial y}\right|_{\varphi(y)=\varphi_{sb}} = |E_b|$, where E_b is the electric field at the buried oxide-substrate interface, as shown in Figure 2-2, and using this identity in Eqs. (9) and (10), we get

$$\left[\left.\frac{\partial\varphi(y)}{\partial y}\right|_{\varphi(y)=\varphi(y)}\right]^2 - |E_b|^2 = \frac{2qN_{ch}}{\varepsilon_{Si}}\left(\varphi(y)-\varphi_{sb}\right) \quad \text{..... (11)}$$

$$|E_b|^2 = \frac{2qN_{ch}}{\varepsilon_{Si}}\left(\varphi_{sbulk}\right) \quad \text{..... (12)}$$

Applying the Poisson equation in the charge-free buried oxide region, we obtain the value of E_b as

$$|E_b| = \frac{\left(\varphi_{sb}-\varphi_{sbulk}\right)}{t_{box}}\frac{\varepsilon_{box}}{\varepsilon_{Si}} \quad \text{..... (13)}$$

By substituting the value of E_b from Eq. (13) in Eqs. (11) and (12), and then, integrating Eq. (11) from the front oxide–silicon film interface $[\varphi(y)=\varphi_{sf}]$ to the buried oxide-silicon film interface $[\varphi(y)=\varphi_{sb}]$, the following equations are obtained:

$$\varphi_{sf} - \varphi_{sb} = \alpha + (\varphi_{sb} - \varphi_{sbulk})\frac{C_{box}}{C_{soi}} \quad \text{..... (14)}$$

$$\varphi_{sb} = \varphi_{sbulk} + \gamma_{bulk}\sqrt{\varphi_{sbulk}} \quad \text{..... (15)}$$

where $\gamma_{bulk} = \frac{\sqrt{2qN_{sub}\varepsilon_{Si}}}{C_{box}}$, $\alpha = \frac{qN_{ch}t_{soi}^2}{2\varepsilon_{Si}}$, $C_{soi} = \frac{\varepsilon_{ox}}{t_{soi}}$ and $C_{box} = \frac{\varepsilon_{ox}}{t_{box}}$.

Equations (6), (14) and (15) together describe the exact Poisson equation for an FDSOI MOSFET and are obtained without any approximation except the assumptions that the back silicon surface and the substrate region never go into inversion and that the device always remains in FD condition. These equations can be solved iteratively to get the exact values of all three surface potentials [9].

2.2 Drain Current Model

Pao and Sah's double integral can be simplified to a single integral if the inversion charge density Q can be expressed as a function of φ_{sf}. This is accomplished by the charge-sheet model which is based on the fact that the inversion layer is located very close to the silicon surface like a thin sheet of charge. There is an abrupt increase of the field (spatial integration of volume charge density) across the thin inversion layer, but very little change of the potential (spatial integration of field) [11].

As shown in the example in Figure 2-3, neither the surface potential nor the depletion charge density changes much after strong inversion. The central assumption of the charge-sheet model for the depletion charge density,

$$Q_d = -qN_aW_d = -\sqrt{2\varepsilon_{Si}qN_a\varphi_{sf}} \quad \text{..... (16)}$$

can be extended to beyond strong inversion. Since the total silicon charge density Q_s is given by

$$V_{GS} = V_{FB} + \varphi_{sf} - \frac{Q_s}{C_{ox}} \quad \text{..... (17)}$$

Now Eq. (16) allows the inversion charge density to be expressed as

$$Q_i = Q_s - Q_d = -C_{ox}\left(V_{GS} - V_{FB} - \varphi_{sf}\right) + \sqrt{2\varepsilon_{Si} q N_a \varphi_{sf}} \quad \text{..... (18)}$$

It should be noted that the charge sheet model does not literally assume all the inversion charge is located at the silicon surface with a zero depth. That would mean $\frac{d|Q_i|}{dV_{GS}} = C_{ox}$ which is not the case with Eq. (18) since φ_{sf} also increase with V_{GS} as described by Eq. (17).

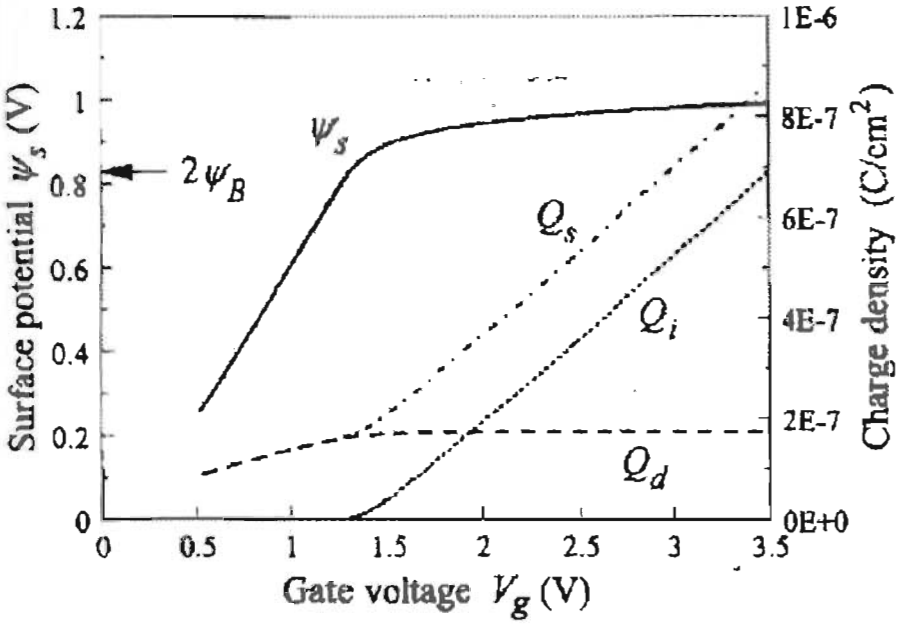

Figure 2-3: Numerical solutions of surface potential (ψ_s), total silicon charge density (Q_s), inversion charge density (Q_i), and depletion charge density (Q_d).

(The MOS device parameters are $N_a = 10^{17}$ cm^{-3}, $t_{ox} = 10$ nm, and $V_{FB} = 0$) [11]

The variable in the drain current integral,

$$I_{ds} = \mu_{eff} \frac{W}{L} \int_0^{V_{DS}} \left(-Q_i(V)\right) dV \quad \text{..... (19)}$$

can be transformed from V to φ_{sf},

$$I_{ds} = \mu_{eff} \frac{W}{L} \int_{\varphi_{ss}}^{\varphi_{sd}} \left(-Q_i(\varphi_{sf})\right) \frac{dV}{d\varphi_{sf}} d\varphi_{sf} \quad \text{..... (20)}$$

where φ_{ss}, φ_{sd} are the values of the surface potential at the source and the drain ends of the channel. For given V_{GS} and V_{DS}, they can be solved numerically from the three surface potentials model by setting $V_{CB} = 0$ for φ_{ss} and $V = V_{DS}$ for φ_{sd} in Eq. (17). Equation (17) can also be used to solve for $V(\varphi_{sf})$

$$V = \varphi_{sf} - \frac{kT}{q} \ln\left\{ \frac{N_a^2}{n_i^2} \left[\frac{C_{ox}^2 \left(V_{GS} - V_{FB} - \varphi_{sf}\right)^2}{2\varepsilon_{Si} kTN_a} - \frac{\varphi_{sf}}{kT} \right] \right\} \quad \text{..... (21)}$$

And evaluate its derivative

$$\frac{dV}{d\varphi_{sf}} = 1 + \frac{2kT}{q} \frac{C_{ox}^2 \left(V_{GS} - V_{FB} - \varphi_{sf}\right) + \varepsilon_{Si} qN_a}{C_{ox}^2 \left(V_{GS} - V_{FB} - \varphi_{sf}\right)^2 - 2\varepsilon_{Si} qN_a \varphi_{sf}} \quad \text{..... (22)}$$

Substituting Eqs. (18) and (22) into Eq. (20) yields [11]

$$I_{ds} = \mu_{eff} \frac{W}{L} \int_{\varphi_{ss}}^{\varphi_{sd}} \left[\begin{array}{l} C_{ox} \left(V_{GS} - V_{FB} - \varphi_{sf}\right) - \sqrt{2\varepsilon_{Si} qN_a \varphi_{sf}} \\ + \dfrac{2kT}{q} \dfrac{C_{ox}^2 \left(V_{GS} - V_{FB} - \varphi_{sf}\right) + \varepsilon_{Si} qN_a}{C_{ox} \left(V_{GS} - V_{FB} - \varphi_{sf}\right) - \sqrt{2\varepsilon_{Si} qN_a \varphi_{sf}}} \end{array} \right] d\varphi_{sf} \quad \text{..... (23)}$$

It is too tedious to carry out the integral in Eq. (23) exactly. A second approximation is introduced in the charge sheet model to obtain an analytical expression for the drain current. The first two terms in the square bracket of Eq. (23) is simply $-Q_i$. Because of the $\frac{kT}{q}$ multiplier, the last term in the square brackets is usually much smaller than the first two unless $Q_i \approx 0$

which happens when $C_{ox}(V_{GS}-V_{FB}-\varphi_{sf})\approx\sqrt{2\varepsilon_{Si}}$. It is then a good approximation to apply this equation to the last term in the square brackets so that the integral can be carried out analytically [11]

$$I_D=\mu_{eff}\frac{W}{L}\left\{C_{ox}\left(V_{GS}-V_{FB}+\frac{kT}{q}\right)\varphi_{sf}-\frac{1}{2}C_{ox}\varphi_{sf}^2-\frac{2}{3}\sqrt{2\varepsilon_{Si}qN_{ch}}\varphi_{sf}^{\frac{3}{2}}+\frac{kT}{q}\sqrt{2\varepsilon_{Si}qN_{ch}\varphi_{sf}}\right\}\Bigg|_{\varphi_{ss}}^{\varphi_{sd}}$$

..... (24)

2.3. Surface Electric Field and Surface Charge

One of the key equations governing the operation of VLSI devices is Poisson's equation. It comes from Maxwell's first equation, which in turn is based on Coulomb's law for electrostatic force of a charge distribution. Poisson's equation is expressed in terms of the electrostatic potential, which is defined as the potential energy of carriers divided by the electronic charge q. The potential energies of carriers are either at the conduction-band edge or at the valence-band edge. Since one is only interested in the spatial variation of the electrostatic potential, it can be defined with an arbitrary additive constant. It makes no difference whether E_c, E_v or any other quantity displaced from the band edges by a fixed amount is used to represent the potential. Conventionally, the electrostatic potential is defined in terms of the intrinsic Fermi level,

$$\varphi_i=-\frac{E_i}{q} \quad \text{..... (25)}$$

There is a negative sign because E_i is defined as electron energy while φ_i is defined for a positive charge. The band diagram can thus be considered also as a potential diagram with the potential increasing downward, opposite to the electron energy [11].

The electric field E_s which is defined as the electrostatic force per unit charge is to the negative gradient of φ .

$$E_s = -\frac{d\varphi}{dy} \quad \text{..... (26)}$$

Now we can write Poisson's equation as

$$\frac{d^2\varphi}{dy^2} = -\frac{dE_s}{dy} = -\frac{\rho_{net}(y)}{\varepsilon_{Si}} \quad \text{..... (27)}$$

Where $\rho_{net}(y)$ is the net charge density per unit volume at y, and ε_{Si} is the permittivity of silicon equal to $11.7\varepsilon_0$. Here $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm is the vacuum permittivity [11].

Another form of Poisson's equation is Gauss's law, which is obtained by integrating Eq. (27)

$$E_s = \frac{1}{\varepsilon_{Si}} \int \rho_{net}(y)dy = \frac{Q_s}{\varepsilon_{Si}} \quad \text{..... (28)}$$

where Q_s is the integrated charge density per unit area. Now the surface charge can be obtained from Eq. (17) if φ_{sf} is known

$$Q_S = -C_{ox}\left(V_{GS} - V_{FB} - \varphi_{sf}\right) \quad \text{..... (29)}$$

Therefore the surface electric field becomes [11]

$$E_S = -\frac{C_{ox}}{\varepsilon_{Si}}\left(V_{GS} - V_{FB} - \varphi_{sf}\right) \quad \text{..... (30)}$$

2.4. Capacitances of MOS Structure

We now consider the capacitances of a MOS structure. In most cases, MOS capacitances are defined as small-signal differential of charge with respect to voltage or potential. They can easily be measured by applying a small ac voltage on top of a dc bias across the device and measuring the out-of-phase ac current at the same frequency (the in-phase component gives the small-signal conductance). The total MOS capacitance per unit area is [11]

$$C_g = \frac{d(-Q_s)}{dV_g} \quad \text{..... (31)}$$

By substituting the value of Q_s, we get

$$C_g = C_{ox}\left\{\frac{\rho(\varphi_{sf})^{\frac{1}{2}}}{\rho(\varphi_{sf})^{\frac{1}{2}} + k_0 \frac{q}{kT}\left(1+\frac{n_i^2}{N_A^2}e^{\frac{q\varphi_{sf}}{kT}}\right)}\right\} \quad \text{..... (32)}$$

where $\rho(\varphi_{sf}) = \frac{q}{kT}\varphi_{sf} + \frac{n_i^2}{N_A^2}e^{\frac{q\varphi_{sf}}{kT}}$

Then the normalized gate capacitance is

$$\frac{C_g}{C_{ox}} = \frac{\rho(\varphi_{sf})^{\frac{1}{2}}}{\rho(\varphi_{sf})^{\frac{1}{2}} + k_0 \frac{q}{kT}\left(1+\frac{n_i^2}{N_A^2}e^{\frac{q\varphi_{sf}}{kT}}\right)} \quad \text{..... (33)}$$

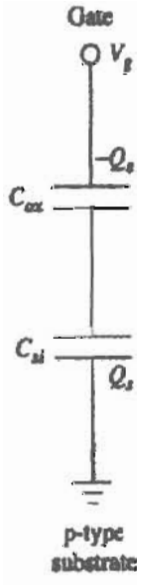

Figure 2-4: Equivalent circuits of an MOS capacitor with all the silicon capacitances are lumped into C_{si}

In other words, the total capacitance equals the oxide capacitance and the silicon capacitance connected in series. The capacitances are defined in such a way that they are all positive quantities. An equivalent circuit is shown in Figure 2-4. In reality, there is also an interface trap capacitance in parallel with C_{Si}. It arises from charging and discharging of Si-SiO_2 interface traps [11].

3. SIMULATED RESULTS AND DISCUSSIONS

The simulation results and performance comparison between SOI and InAs XOI MOSFETs are discussed in this chapter. The model uses three surface potentials as discussed in Ref. [9]. However, before we proceed, first we verify our model with the results of Ref. [9]. For this, we generate the three surface potentials of a SOI MOSFETs with the same parameter set that is used in Ref. [9]. Figure 3-1 and 3-2 shows the variation of surface potentials φ_{sf}, φ_{sb} and φ_{sbulk} versus the gate voltage of SOI MOSFET for a front oxide thickness of 3 nm, buried oxide thickness of 100 nm and silicon film thickness of 50 nm. The silicon film doping is kept sufficiently high 1×10^{17} cm^{-3} to ensure the absence of channel at the back silicon layer surface.

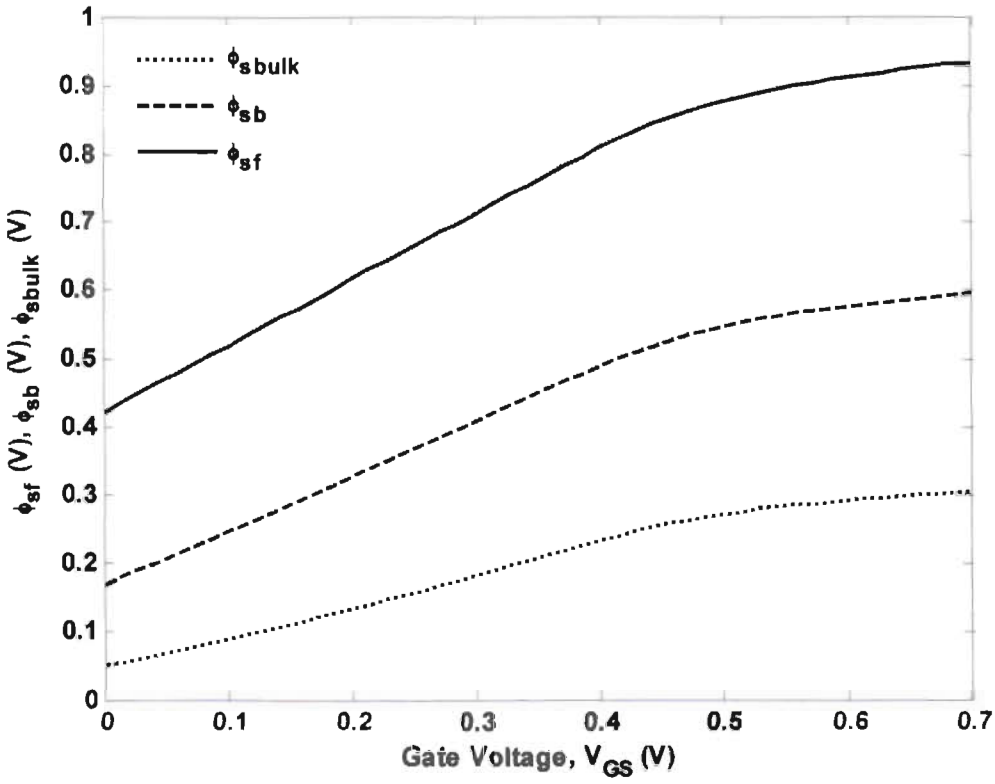

Figure 3-1: Different Surface Potential versus Gate Voltage Curve

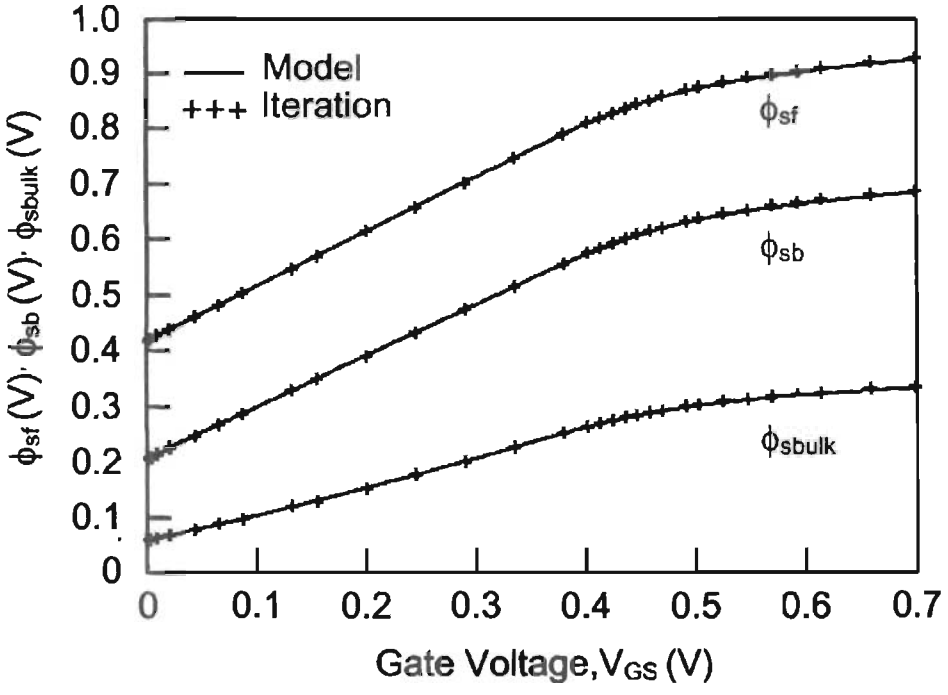

Figure 3-2: Different Surface Potential versus Gate Voltage Curve [9]

The substrate doping is selected quite low 1×10^{15} cm^{-3} to clearly demonstrate the effect of substrate depletion charge on the front surface potential. When the substrate doping is low, a large potential drop appears across the substrate depletion region, which changes the channel inversion charge density significantly. The results of Ref. [9] are shown in Figure 3-2. A comparison between Figures 3-1 and 3-2 indicates that our model (code) is producing correct results.

3.1. Performance Comparison between SOI and XOI MOSFET

The three surface potential based compact model is used to generate the surface potentials and then the front surface potential is used to calculate the I-V and C-V curves for performance comparison between the SOI and XOI MOSFETs. The different parameters used for the InAs XOI MOSFET are shown in Table 1. These parameters have been used in Ref. [12]. For fair comparison, the same device dimensions and doping densities are assumed for the SOI MOSFET.

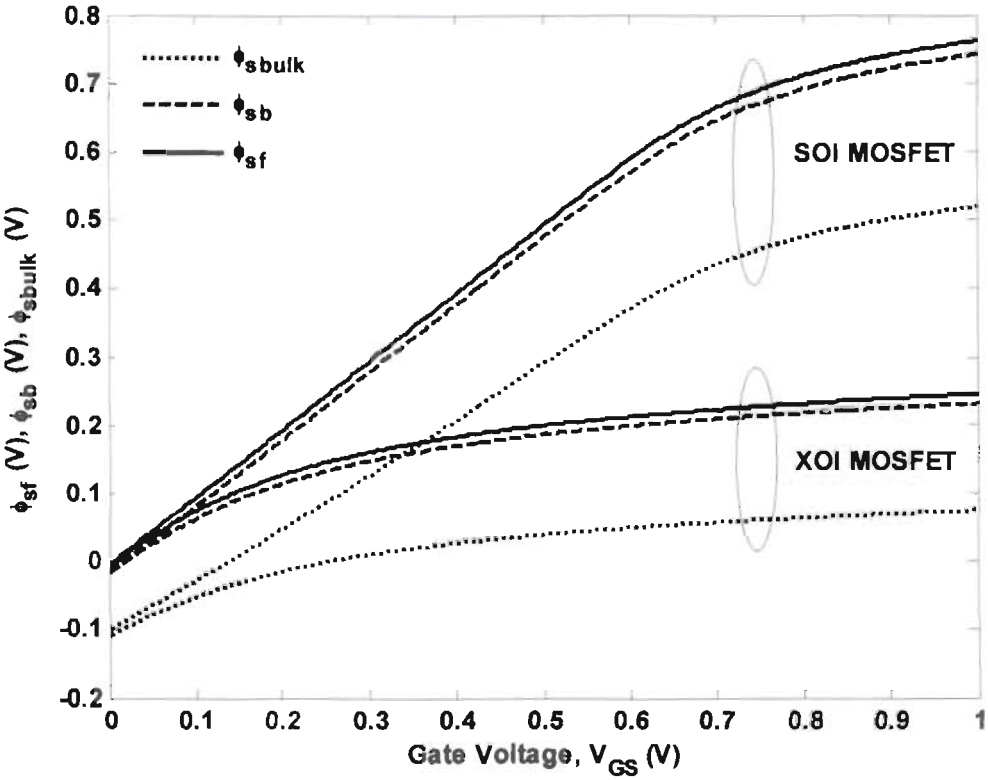

Figure 3-3: Different surface potentials versus gate voltage curve

Figure 3-3 shows the variation of surface potentials φ_{sf}, φ_{sb} and φ_{sbulk} versus the gate voltage of SOI and XOI MOSFETs for a front oxide thickness of 7 nm, buried oxide thickness of 50 nm and silicon film thickness of 15 nm. Here, the surface potential curves of XOI MOSFET are saturated quicker than SOI MOSFET. We have got small saturation value of front surface potential because a large potential drops across the gate oxide and a smaller voltage drops across the channel thickness of XOI MOSFET.

Table 1: Simulation parameters of SOI and XOI MOSFETs [12]

Subject	SOI	XOI
Flat Band voltage, V_{fb}	-0.2 V	-0.2V
Electron concentration in channel, N_{ch}	4×10^{16} cm^{-3}	4×10^{16} cm^{-3}

Electron concentration in substrate, N_{sub}	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}
Intrinsic concentration, n_i	1.5×10^{10} cm^{-3}	1×10^{15} cm^{-3}
Gate Oxide thickness, t_{ox}	7 nm	7 nm
Buried Oxide thickness, t_{box}	50 nm	50 nm
Channel Thickness, t_{soi}	15 nm	15 nm
Vacuum Permittivity, ε_o	8.854×10^{-12} F/m	8.854×10^{-12} F/m
Relative permittivity of silicon dioxide, $\varepsilon_{r,ox}$	3.9	3.9
Relative permittivity of Zirconium dioxide, $\varepsilon_{r,zr}$	20	20
Electron mobility, μ_e	650 cm^2/V-s	1300 cm^2/V-s
Channel Length, L	500 nm	500 nm

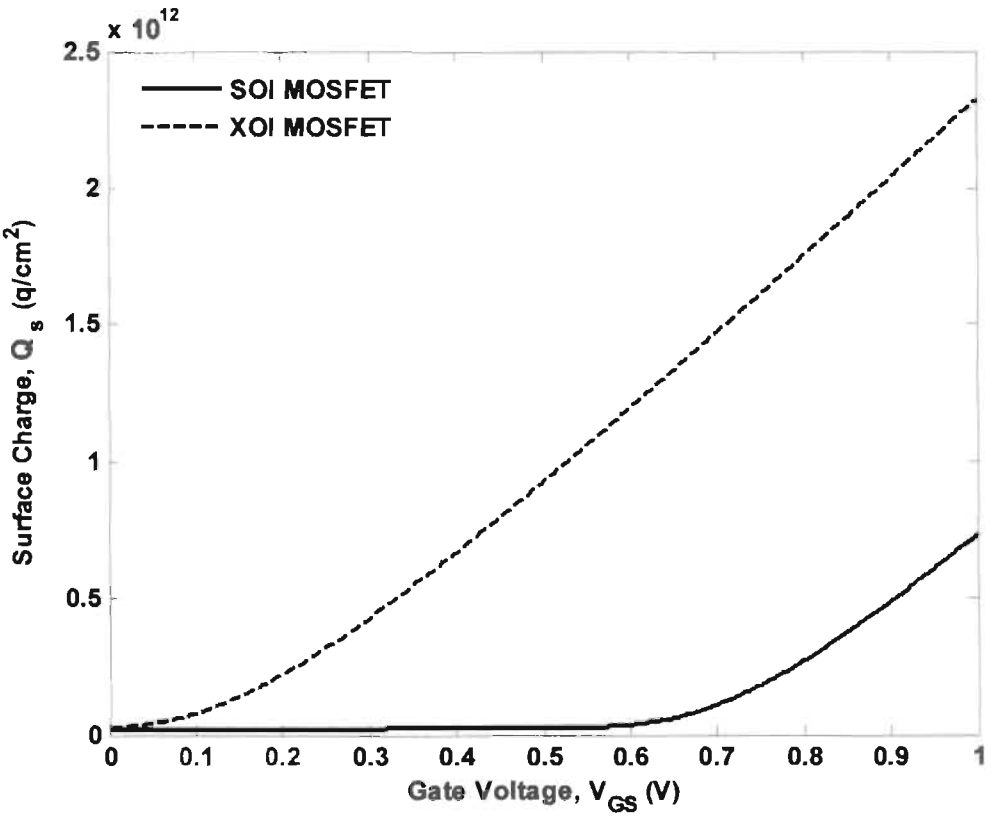

Figure 3-4: Surface charge versus gate voltage curve

Figure 3-4 shows the surface charge density versus gate voltage curve between SOI and XOI MOSFETs. There are two regions of the curve. The flattened region represents the weak inversion region and the rising part is the strong inversion region. Since the inversion charge density increases rapidly with an increase in gate voltage as we have seen in the Figure 3-4. It occurs like that the surface potential changes with gate voltage and the electron concentration increases rapidly with very small changes in surface potential. We have observed, for XOI MOSFET the surface charge curve reaches in strong inversion region earlier than SOI MOSFET. For this, the surface potentials of XOI MOSFET saturated earlier than SOI MOSFET.

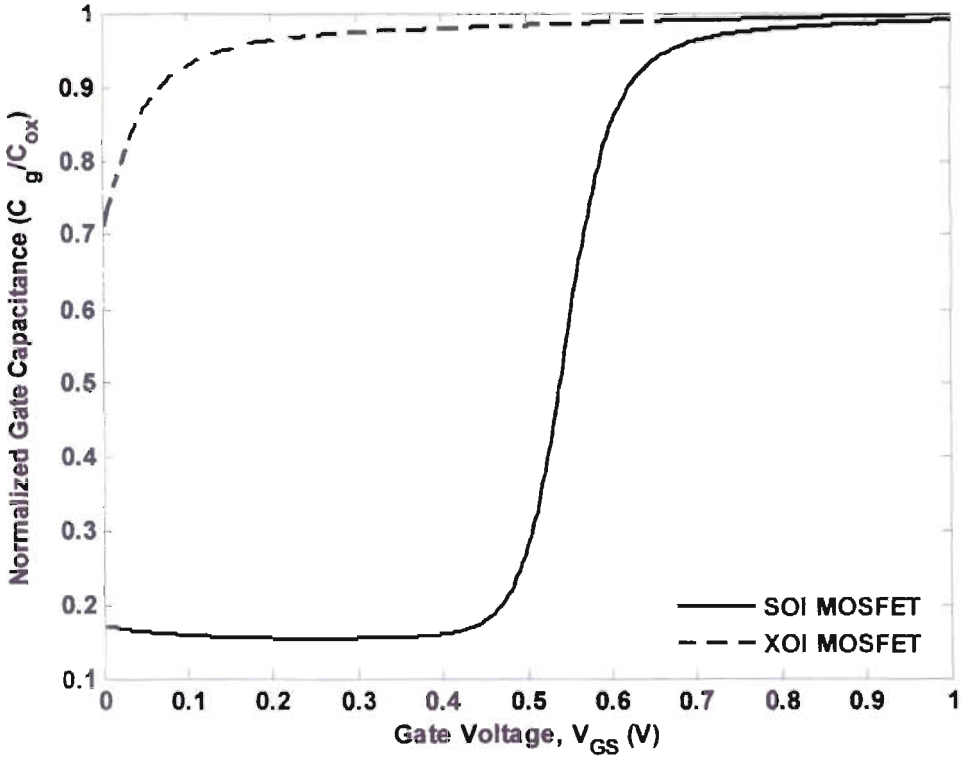

Figure 3-5: Gate capacitance versus gate voltage curve

Figure 3-5 shows the normalized gate capacitance (C_g / C_{ox}) vs. gate voltage (V_{GS}) curve between SOI MOSFET and XOI MOSFET. If we increase gate voltage, the gate capacitance will be flattened. There are two regions in the curve. The rising part of this curve is weak inversion

region and the flattened part is strong inversion region. For SOI MOSFET at first the curve is flat and the capacitance value is small because the FET turns on at $V_{GS} \approx 0.45$ V. After the FET is turned on, the capacitance rapidly increases with gate bias and saturates to C_{ox} at strong inversion. The gate capacitance of the XOI FET quickly saturates to C_{ox} because the XOI FET turns on at a very small gate bias.

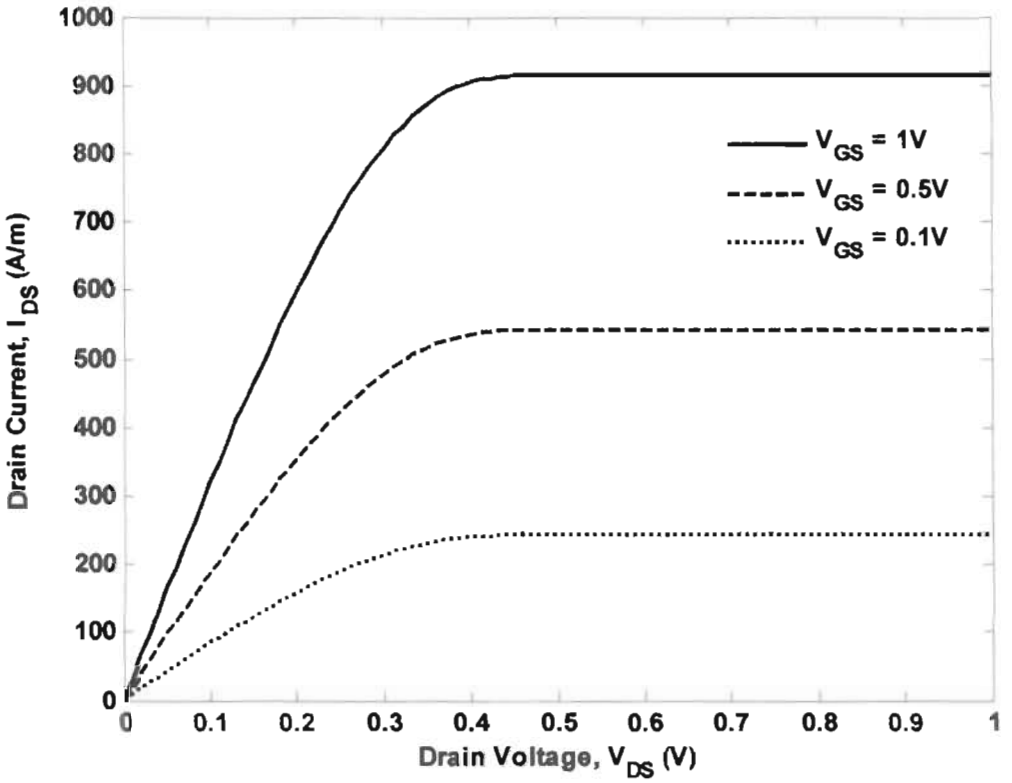

Figure 3-6: I_D versus V_{DS} characteristic curve of SOI MOSFET for different gate voltage

Figure 3-6 and Figure 3-7 show $I_D - V_{DS}$ characteristics curves of SOI and XOI MOSFETs respectively for different gate voltages. When V_{GS} changes, the I_D versus V_{DS} curve will change. We saw that, if V_{GS} increases, the initial slope of I_D versus V_{DS} increases. The drain current in saturation is virtually independent of V_{DS} and the MOSFET acts as a current source. This is because there is no carrier inversion at the drain region of the channel. Carriers are pulled into the high electric field and ejected out of the drain terminal. The drive current of

XOI MOSFET is almost 6 times higher than SOI MOSFET. So, we have got better output current from XOI MOSFET.

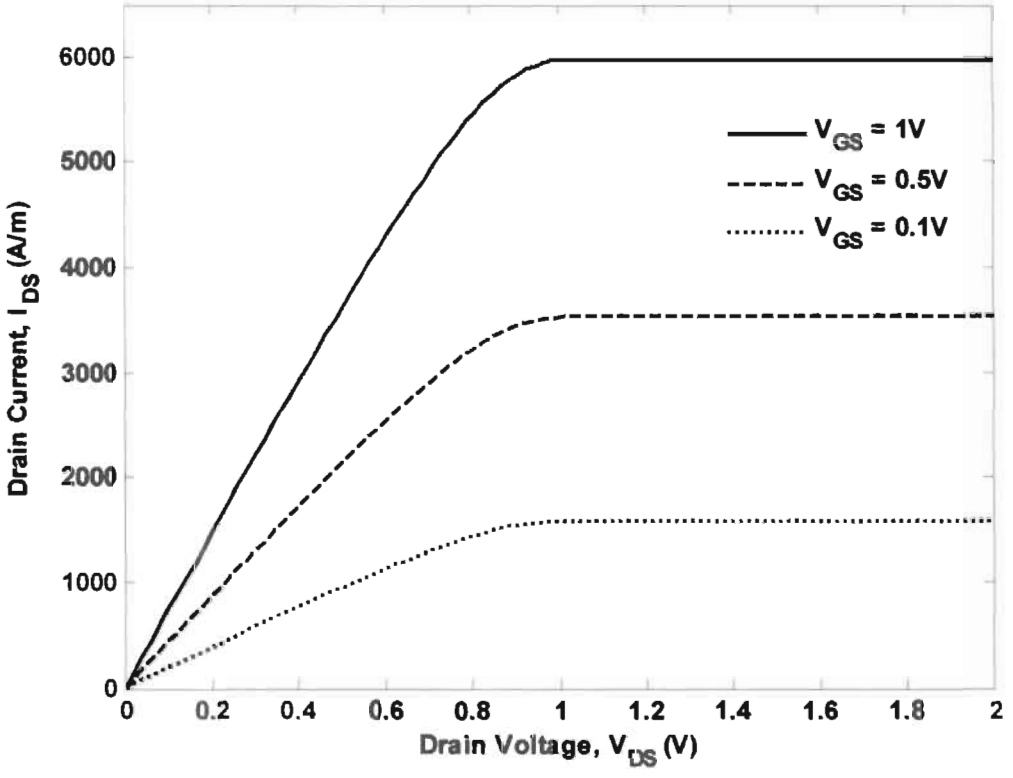

Figure 3-7: I_D versus V_{DS} characteristic curve of XOI MOSFET for different gate voltage

Figure 3-8 and Figure 3-9 show the $I_D - V_{GS}$ characteristics curves of SOI and XOI MOSFETs respectively for V_{DS} = 1V. For SOI MOSFET, after around 0.55V the we get current, that means the transistor becomes on. And for XOI MOSFET, after around 0.05V we get current, that means the transistor becomes on. Here the XOI MOSFET current is 6 times higher than XOI MOSFET.

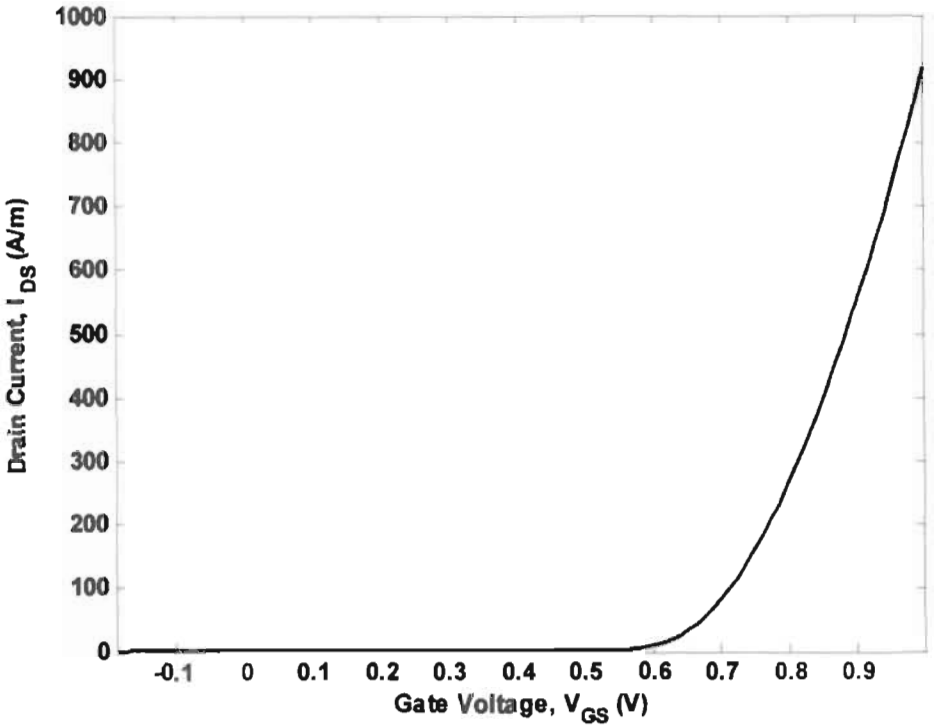

Figure 3-8: I_D versus V_{GS} characteristics curve of SOI MOSFET (For V_{DS} = 1V)

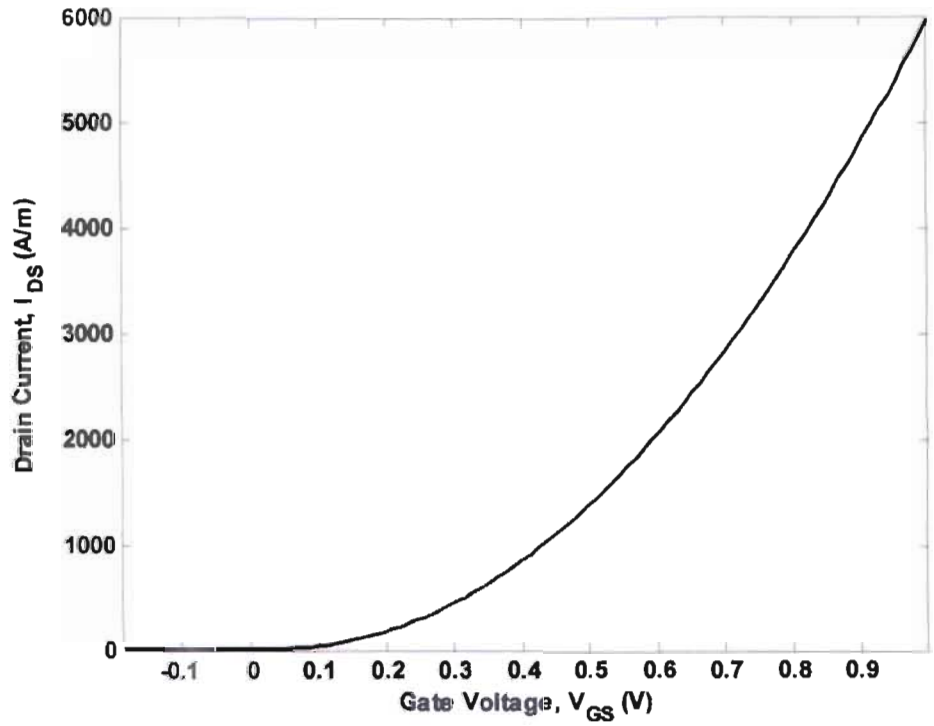

Figure 3-9: I_D versus V_{GS} characteristics curve of XOI MOSFET (For V_{DS} = 1V)

Figure 3-10 shows the $I_D - V_{GS}$ characteristics curve of SOI MOSFET for V_{DS} = 1V. From this curve, we can calcuate the threshold voltage (V_{th}) and ON current (I_{ON}).

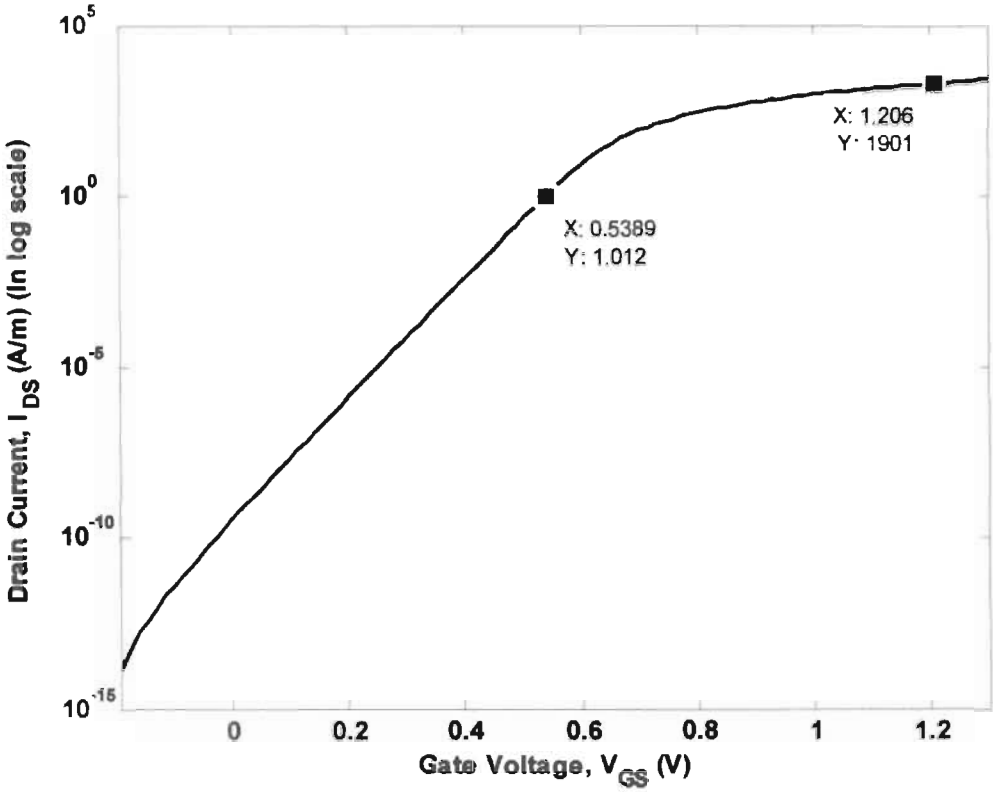

Figure 3-10: I_D versus V_{GS} characteristics curve of SOI MOSFET (For V_{DS} = 1V) (In log scale)

Threshold voltage is the gate voltage at which the drain current is 1 A/m. Here, we see that the threshold voltage V_{th} = 0.5389 V. Now the on current will be the drain current at ON voltage $V_{ON} = V_{th} + \left(\frac{2}{3}\right)V_{DD}$. Here, V_{DD} =1V. So, V_{ON} = 1.2056 V and thus the ON current I_{ON} = 1901 A/m.

Figure 3-11 shows the $I_D - V_{GS}$ characteristics curve of XOI MOSFET for V_{DS} = 1V. Here is also the current of XOI MOSFET is 6 times higher than the SOI MOSFET. From this curve, we can calcuate the threshold voltage (V_{th}) and ON current I_{ON}. Here, we see that the threshold voltage V_{th} = -0.02632 V. This voltage is negative. That's why the MOSFET will

remain on without applying any gate voltage. So, this XOI MOSFET is an ON transistor. Now the on current will be the drain current at ON voltage $V_{ON} = V_{th} + \left(\frac{2}{3}\right)V_{DD}$. Here, V_{DD}=1V. So, V_{ON} = 0.6403 V and thus the ON current I_{ON} = 2367 A/m which is around 1.2 times higher than SOI MOSFET.

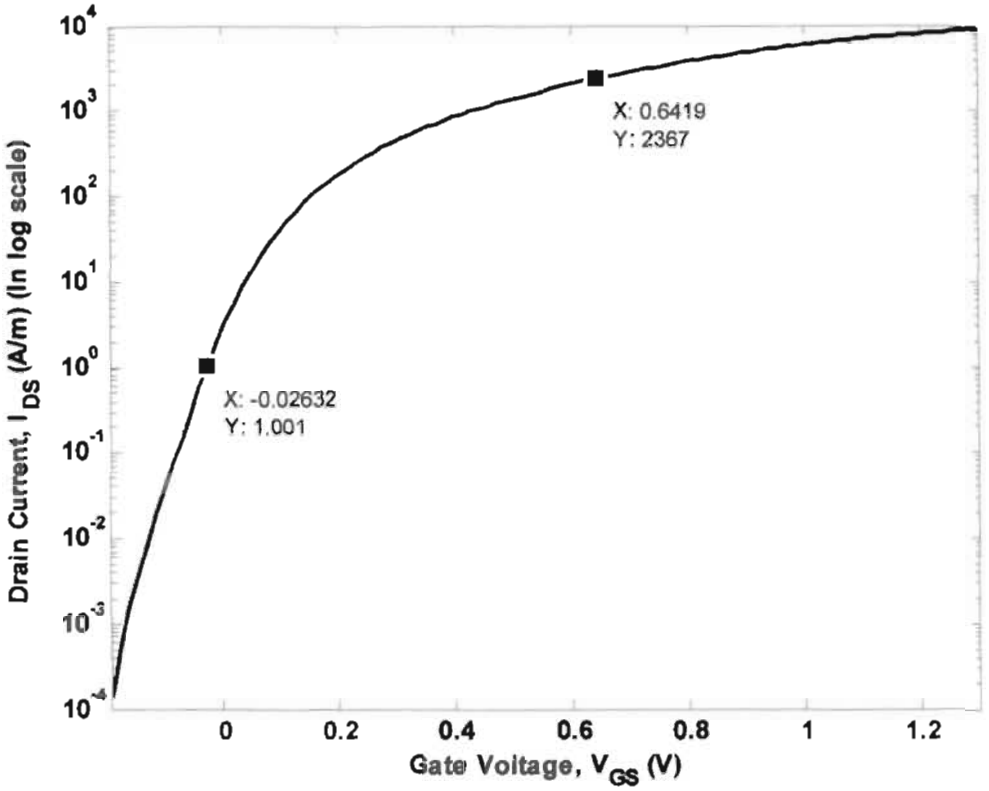

Figure 3-11: I_D versus V_{GS} characteristics curve of XOI MOSFET (For V_{DS} = 1V) (In log scale)

Figure 3-12 shows the transconductance versus gate voltage characteristics curve for SOI and XOI MOSFETs for V_{DS} = 0.5 V and L = 500 nm. The MOSFET transconductance is defined as the change in drain current with respect to the corresponding change in gate voltage. The transconductance increaes linearly with V_{DS} but is independent of V_{GS} in the saturation region. The transconductance is also a function of the geometry of the device as well as of carrier mobility and threshold voltage. For XOI MOSFET, transconductance is around 1.2 times higher than that of SOI MOSFET. This is because the carrier mobility of InAs is higher than that of Si.

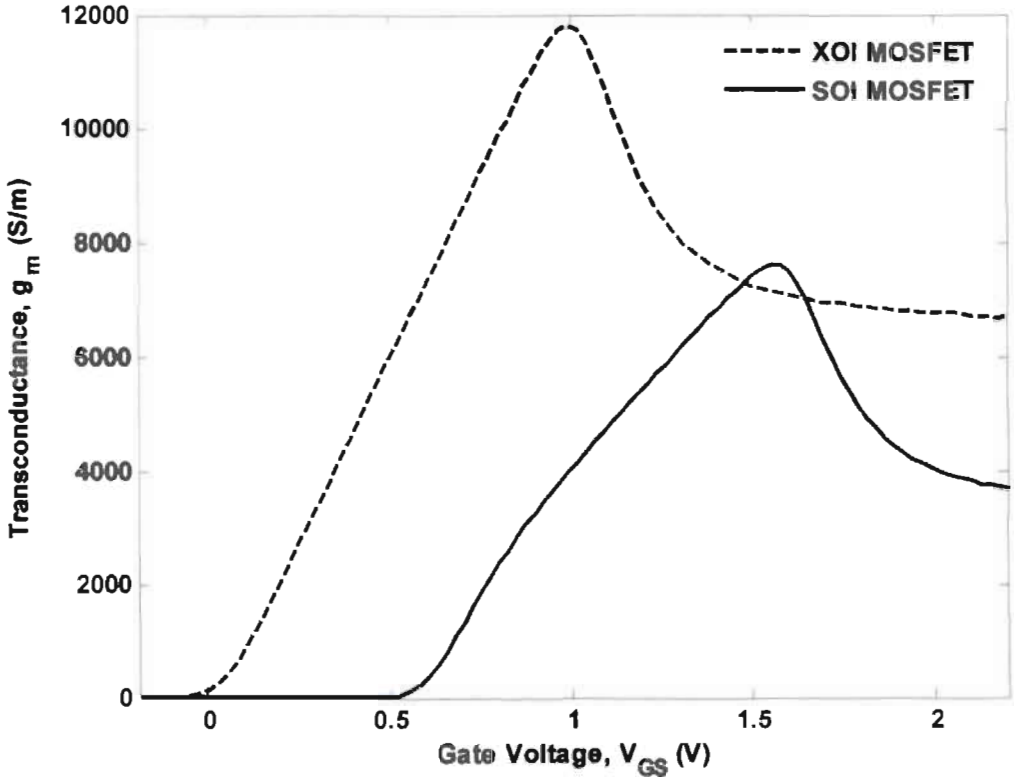

Figure 3-12: Transconductance versus Gate voltage curve of SOI MOSFET

Figure 3-13 shows the unity gain frequency versus gate voltage characteristics curve of XOI and SOI MOSFETs. The unity gain frequency of a MOSFET (f_T) is defined as the frequency at which the short-circuit current-gain (i_d / i_g) of the common-source amplifier becomes unity. f_T is also called the transition frequency. f_T gives an idea of the high-frequency behavior of the MOSFET.

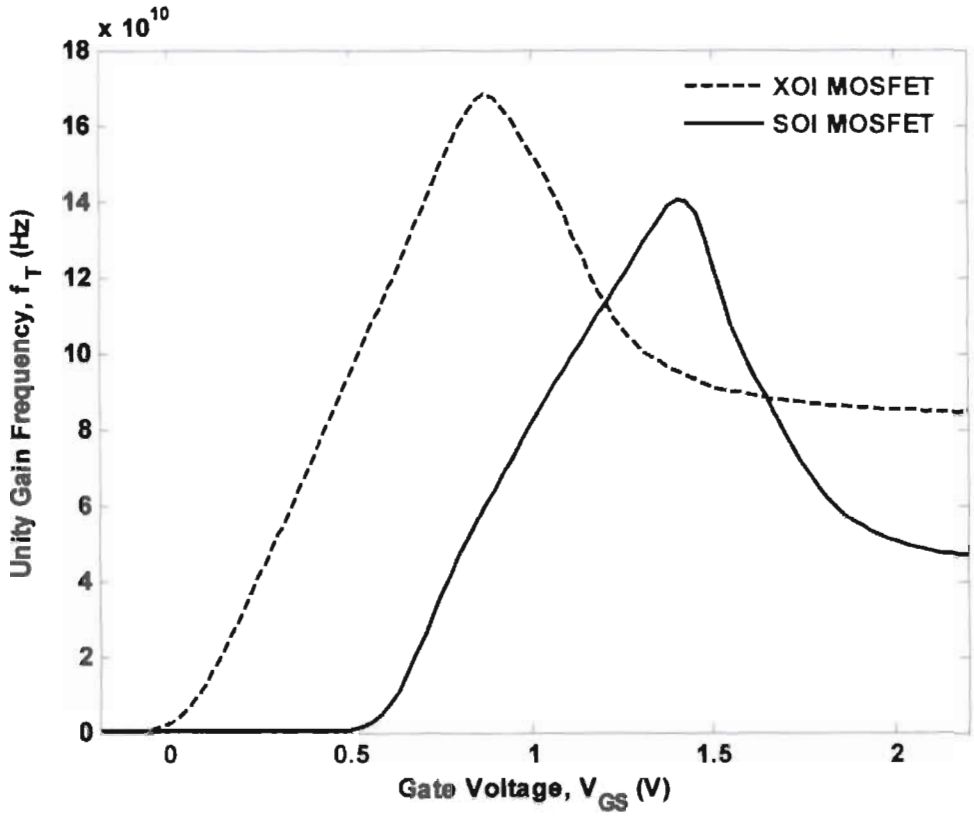

Figure 3-13: Unity gain frequency versus gate voltage curve of SOI MOSFET

In XOI MOSFET, unity gain frequency f_T is 1.2 times higher than SOI MOSFET. Higher f_T means higher transconductance and lower internal MOSFET capacitances which means better amplification. So, by using XOI MOSFET, we can amplify signal more than SOI MOSFET.

4. CONCLUSION

We have studied the performance comparison between InAs-on-insulator and Silicon-on-insulator MOSFETs using three surface potentials based compact model. After verification of our model with the Ref. [9], we simulated the different characteristics of SOI MOSFET and then we change the channel material to InAs by replacing Si. We also simulated different characteristics of both MOSFETs. Here we use fully depleted (FD) SOI and XOI MOSFETs as this structure provides better performance such as low threshold voltage, small leakage current and smaller floating body effect over partially depleted (PD) SOI and XOI MOSFETs. The significant changes are observed in surface potential, surface charge density, gate capacitance, drain current, transconductance and unity gain frequency. The output characteristic shows a better performance for InAs than SOI. We have got high drain current, transconductance and unity gain frequency of XOI MOSFET. From the simulation results, we observe that, for the same device dimensions and doping densities of the SOI and XOI MOSFETs, we got around 6 times higher drive current, around 1.5 times higher transconductance and around 1.2 times higher unity gain frequency. On the other hand, we got very low (negative) threshold voltage for XOI MOSFET. After the analysis, we see that, to overcome the limitations of bulk silicon MOSFET, we can use SOI MOSFET which can be solved the scaling problems. And over SOI MOSFET, XOI MOSFET has better performance because of high carrier mobility of compound semiconductors such as III-V semiconductors. So, by using XOI MOSFET, we can get high speed operation and amplification, low power consumption than SOI MOSFET as well as bulk silicon MOSFET.

5. FUTURE WORK

5.1. Quantum Mechanics

MOSFETs fabricated on an III-V on-insulator (XOI) substrate with an extremely thin XOI layer have attracted a great deal of attention, in part because of their better immunity to short-channel effects. To enhance this immunity, the thickness of the XOI layer should be from about one-third to one-fourth the gate length. For instance, it should be 5-6 nm when the gate length is 20 nm. When the XOI layer is 10 nm thick or less, the device is called an ultrathin-body XOI MOSFET. On the other hand, the envelope function of the inversion-layer electrons in bulk MOSFETs has a width of approximately 10-20 nm. As a result, electrons in an ultrathin (5-6 nm) XOI layer are strongly confined by the gate oxide and the buried oxide, thus bringing quantum mechanical effects into play [13]. In future, we want to incorporate this quantum mechanical effect in our XOI MOSFETs model to observe the different characteristics for better improvement.

5.2. D_{it} (Interface trap density) Effect

Some nonideal effects can be incorporated in the model such as: fixed charges, trapped charges in oxides and non-zero semiconductor-metal or poly-Silicon barrier heights. There are two major electrical properties of the InAs-ZrO_2 interface which must be considered. They are: fixed charge and interface trap density (D_{it}). Fixed oxide charges affect the device performance if present in high densities. Interface traps also pose a stability problem since trapped charge density can change during device operation. Carrier scattering induced by an interface trapped charge, whose density depends on the gate voltage. Interface states induce stretching of the C-V curve, because the trap charge density depends on the Fermi level at the InAs-ZrO_2 and consequently on the applied gate voltage. Interface trap charges are positively or negatively charged. These are located within the InAs forbidden gap at the InAs-ZrO_2. Unlike a fixed oxide

charge, an interface trapped charge interacts strongly with the underlying InAs and can thus be charged or discharged depending on the surface potential [14]. So, we want to include this effect in future to improve XOI MOSFET performance.

6. REFERENCES

[1] Narayana Murty Kodeti, "White paper on Silicon-on-insulator (SOI) implementation", *Infotech Enterprises Ltd.*, pp. 3-8, June 2009

[2] Takayasu Sakurai, Akira Matsuzawa, and Takakuni Douseki, "Fully depleted SOI CMOS circuits and technology for ultra-low power applications", *First edition, Springer,* ch. 1, pp. 1-19, 2006

[3] John Z. Ren, "Low voltage SOI MOSFET with suppressed floating body effects", *Master of Applied Science thesis paper, University of Toronto*, pp. 9-17, 1999

[4] Aatish Kumar, V. Ramgopal Rao and Rakesh Lal, "Simulation and characterization of SOI MOSFETs", *Dual degree project report, Indian Institute of Technology, Mumbai*, pp. 49-50, 2001

[5] *http://en.wikipedia.org/wiki/SiliconOnInsulator*

[6] Zhou Xing and Lim Khee Yong, "A general approach to compact threshold voltage formulation based on 2D numerical simulation and experimental correlation for deep submicron ULSI technology development", *IEEE Transactions on Electron Devices*, vol. 47, pp. 214-221, January 2000

[7] Neil H. E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", *Second edition, Addison Wesley*, ch. 2, pp. 27-35, October 1994

[8] Haldun Haznedar, "Digital Microelectronics", *First edition, Benjamin-Cummings publication company*, ch. 5, pp. 174-181, January 1991

[9] Pradeep Agarwal, Govind Saraswat, and M. Jagadesh Kumar, "Compact surface potential model for FD SOI MOSFET considering substrate depletion region", *IEEE Transactions on Electron Devices*, vol. 55, no. 3, pp. 789-795, March 2008

[10] J. R. Brews, "A charge-sheet model of the MOSFET," *Solid State Electron.*, vol. 21, pp. 345-346, 1978

[11] Yuan Taur and Tak H. Ning, "Fundamentals of modern VLSI devices," *Second edition, Cambridge University Press*, ch. 2-3, pp. 52-90, 2009

[12] Hyunhyub Ko, Kuniharu Takei, Rehan Kapadia, Steven Cguang, Hui Fang, Paul W. Leu, Kartik Ganapathi, Elena Plis, Ha Sul Kim, Szu-Ying Cgen, Morten Madsen, Alexandra C. Ford, Yu-Lun Chueh, Sanjay Krishna, Sayeef Salahuddin and Ali Javey, " Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors", *Nature*, vol. 468, pp. 286-289, November, 2010

[13] Takayasu Sakurai, Akira Matsuzawa, and Takakuni Douseki, "Fully depleted SOI CMOS circuits and technology for ultra-low power applications", *First edition, Springer,* ch. 8, pp. 372-373, 2006

[14] Dieter K. Schrodera and Jeff A. Babcock, "Negative bias temperature instability: road to cross in deep submicron silicon semiconductor manufacturing", *Applied Physics Reviews-Focus Review*, pp. 5-6, July 2003