EAST WEST UNIVERSITY

"Study of scaling effects of a double gate silicon MOSFET"

By

Md. Manzurul Hasan

&

Md. Emran Hassan

In partial fulfillment of the requirements for the degree of
Bachelor of Science in Electrical & Electronic Engineering
(B.Sc. in EEE)

Summer, 2015

Department of Electrical & Electronic Engineering
Faculty of science and engineering
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______________________ ______________________

Thesis Advisor
Dr. Khairul Alam

Chairperson
Dr. Halima Begum

Abstract

Nowadays technology keeps progressing and device becomes smaller for fast processing. With small dimensions the quantum mechanical effects become prominent and the device performance degrades due to severe short channel effects such as threshold voltage roll off. We study the device dimensions effects on the performance of a double gate silicon MOSFET using energy balance model with Bohm quantum potential of Silvaco simulation tool. For a 2 nm SiO_2 gate oxide with $10^{19}\ cm^{-3}$source-drain doping density, the device threshold voltage remains constant upto channel length of $\cong$ 40 nm, below which the threshold voltage falls off rapidly. The channel body thickness and oxide thickness affect the threshold voltage when the channel length is below 40 nm. We observe similar dimension effects on sub-threshold swing.

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Authorization page

We hereby declare that we are the sole author of this thesis. We authorize East West University to lend this thesis to other institution or individuals for the purpose of scholarly research.

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Chapter 1

Introduction

The revolutionary improvement of electronics, information technology and communications has mainly done by continuous progress in silicon-based complementary metal-oxide semiconductor (CMOS) technology. Nowadays CMOS IC's are magnificently used in every aspect of our life, ranging from portable electronics to telecommunications and transportation. In 1965 Gordon Moore predicts that the performance of integrated circuit will be doubled after every two years [1]. As predicted by him, continuous down-scaling of the MOSFET transistor dimensions are being done in order to reach higher packing density, performances improvement, faster circuit speed and lower power consumption [2]. However further scaling of CMOS devices may cause several drawbacks like, increasing leakage current, which does not allow further reduction of threshold voltage, and the consequence is to prevent further supply voltage scaling for the historical speed improvement. This drawback makes attention towards engineers to make the structural modification of the device. In double gate MOSFET it incorporates two symmetrical gates on its top and bottom. The advantages of a double gate MOSFET is, it controls the channel very efficiently which helps to reduce short channel effects and drives higher currents than a MOSFET having single gate.

From last 4 decade, semiconductor device technology has changed with an amazing speed [3]. An exponential improvement of IC's performance is achieved due to down scaling of MOSFET dimensions. Scaling of channel length results in short channel effect like threshold voltage, sub threshold slope, ON current and OFF current which play a major role in determining the performance of scaled devices. The double gate MOSFET's are electro-statically superior to a single gate MOSFET and allows for additional gate length scaling [4].

As scaling is expected to reach the 14 nm era in a few years, the DG MOSFET becomes necessary in terms of its superior properties in this scaling region [5]. International Technology

Roadmap for Semiconductor, devices with gate lengths down to 10 nm can be expected in 2019 [5-6].

To reduce the power, the threshold voltage of the MOSFET has to be reduced. However, as threshold voltage is decreased, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available. Hence sub-threshold leakage current is major issue of modern high-performance VLSI chips [7]. The DG MOSFET's are the devices, which are having two gates on either side of the channel. One in upper side, known as top gate and another one is in the lower side of the channel, known as bottom gate. It gives better control of the channel by the gate electrodes. This ensures that no part of the channel is far away from a gate electrode. The double gate MOSFET (DG MOSFET) structure minimizes short-channel effects that allows more aggressive device downscaling of device up to 10 nm gate length [8].

1.1 Research Objectives

The objective of this work is to study the short channel effects such as threshold voltage, sub threshold slope of a silicon double gate MOSFET. In this thesis work, we studied the performance of a double gate MOSFET by varying channel length, oxide thickness, and silicon body thickness using the industry standard simulation package Silvaco. We also observed the body thickness effect & oxide thickness effect on the performance. For doing this we use Silvaco simulation package. We used *models bqp.n bqp.ngamma=1.2 bqp.nalpha=0.5 bqp.p bqp.pgamma=1.0 bqp.palpha=0.5 srh fermi ni.fermi fldmob hcte evsatmod=0* and *method climit=1.0e-4 block clim.eb=1.0E7 meinr* [9], the details of which are described in chapter 2.

1.2 Literature review

The journey of MOSFET starts from 1960's. From that time it starts a new era of modern electronics. According to Moors law the performance of integrated circuit will be doubled after every two years [1]. For better performance of MOSFET, different types of engineering are implemented on MOSFET. Scaling the oxide thickness may result in tunnel current. Then

engineers move to scale down the channel which gives a better performance. But when channel length, L_G < 30 nm there arises several short channel effects like decrease of threshold voltage, increase of sub-threshold slope, increase of drain induced barrier lowering (DIBL) etc. To mitigate these short channel effects engineers are looking for multi-gate MOSFET like DG MOSFET, Fin-FET, and Vertical MOSFET. These MOSFET's have better performance over bulk MOSFET. Engineers also investigated the behavior (on-off current ratio, sub-threshold swing, drain induced barrier lowering) of double gate MOSFET by varying p-type body doping. The body doping effects are important that need to be considered, for example undopped body of DG MOSFET can avoid the dopant fluctuation effect. This reduces scattering occurred due to impurities [10]. After implementing the DG MOSFET most of the investigation has taken place based on scaling of channel length. Engineers evaluated the variation of the threshold voltage, the sub-threshold slope, the leakage current and the drain-induced barrier lowering. Their investigation shows that channel length is reducing the sub-threshold swing (S) to its ideal value 60 mV/decade.

Nowadays modern IC's are incorporating MOSFET's with channel length in nm region. Robert Dennard's [11] work on scaling theory shows that continuous scale down of MOSFET dimension is possible. In late 2009 Intel began to manufacture MOSFET with less than 32 nm channel length which makes the pace for MOSFET development. Frank, Laux, Fischetti [12] examined double gate Si MOSFET using Monte Carlo simulation. Their results show that the channel length can be reduced down to 30 nm for silicon film having a depth of 5nm and an oxide thickness of 3 nm with an acceptable short-channel effect. Natori examined the double gate MOSFET and its performance using ballistic transport model, and the ballistic results significantly differ from Monte Carlo simulation [13]. Meindi, Chen, and Davis [14] study a double gate MOSFET and show that silicon technology has an enormous potential for terascale integration. They assumed that more than one trillion transistors per chip is feasible by the development of DG MOSFET with gate oxide thickness of about 1 nm.

According to Thompson, Packan, & Bohr [15], the scaling of a double gate MOSFET oxide thickness, source/drain extension (SDE), junction depths, and gate lengths is limited by the tunneling leakage through the SiO_2 below 2.3 nm. Junction depth below 30 nm increases

junction resistance which degrades the MOSFET performance. They propose high-K gate dielectric, low resistive junction and alternate device to overcome those scaling limitations.

1.3 Organization of the thesis

Our thesis report has several chapters which described the whole work. In chapter 1 we discussed the introduction of this thesis along with the objective, literature review, and organization of the paper.

In chapter 2 we make a short description about our models and methods which are incorporated in our program.

In chapter 3, we explain our different results which we obtained from our work. In chapter 4 a conclusion of our thesis work are included.

Chapter 2

Simulation Models and Methods

Device structures are getting smaller day by day and so many short channel effects are introduced due to non local carrier effects. Channel length is the main gauge to predict the effects of non-local carriers and it's being started for gate length less than 40 nm. To accurately solve these effects we need quantum solution. To simulate our silicon DG MOSFET we used bohm quantum potential (BQP) model in our model statements along with energy balance model.

2.1 Introduction of Bohm Quantum Potential (BQP)

BQP model used in ATLAS was first introduced by David Bohm in 1952, which earlier was presented by the name quantum mechanical potential. Later on it was elaborated upon by Bohm and Hiley in its interpretation as an information potential which acts on a quantum particle. In the framework of the de Broglie-Bohm theory quantum potential is a term within Schrödinger equation

$$i\hbar \frac{\partial \psi}{\partial t} = \left(-\frac{\hbar^2}{2m}\nabla^2 + V\right)\psi \tag{2.1}$$

In polar form the wave function can be written as $\psi = R\ \exp(iS/\hbar)$ with real-valued functions R and S, where the wave function ψ has amplitude R and $S/\hbar$ is its phase. From the imaginary and real part of the Schrödinger equation it gives two equations that follow the continuity equation and the quantum Hamilton-Jacobi equation, respectively [16-17].

The imaginary part of the Schrödinger equation in polar form gives

$$\frac{\partial R}{\partial t} = -\frac{1}{2m}\left[R\nabla^2 S + 2\nabla R \cdot \nabla S \right] \tag{2.2}$$

which, has the probability density $\rho = R^2$ and can be interpreted using continuity equation as

$$\frac{\partial \rho}{\partial t} + \nabla \cdot (\rho v) = 0 \tag{2.3}$$

The real part of the Schrödinger equation in polar form yields a modified Hamilton–Jacobi equation

$$\frac{\partial S}{\partial t} = -\left[\frac{(\nabla S)^2}{2m} + V + Q\right] \tag{2.4}$$

also referred to as quantum Hamilton–Jacobi equation [18]. It differs from the classical Hamilton Jacobi equation only by the term Q, where,

$$Q = -\frac{\hbar^2}{2m}\frac{\nabla^2 R}{R} \tag{2.5}$$

This term Q, called quantum potential, thus depends on the curvature of the amplitude of the wave function [19].

2.2 Reason to choose BQP model

Silvaco has introduced different device simulator like, a Schrodinger- Poisson solver and Density Gradient model. The Schrodinger-Poisson (SP) solver is the most accurate approach to calculate the quantum particle movement or quantum particle confinement in semiconductor but it is unable to predict the currents flowing in the device. And to overcome from this limitation, ATLAS provides a Density Gradient (DG) model. It provides a good prediction on both the quantum confinement and the drift diffusion currents along with the Fermi Dirac statistics for a 2D structure. But this model shows poor performance on convergence in 3D and with the hydrodynamic transport.

Therefore Silvaco has introduced in ATLAS, a new approach called bohm quantum potential (BQP). It shows many advantages like, it incorporate two fitting parameters which ensure a good calibration for silicon or non silicon materials, planar or non planar devices. This model shows stable and robust performance numerically and independently used transport model. Those are the reason to choose this model to simulate our device [9].

2.3 Bohm quantum potential (BQP) model in silvaco

The BQP model introduces a position dependent quantum potential assigned by, Q, which is added to the potential energy of a given carrier type. This quantum potential Q is derived using the Bohm interpretation of quantum mechanics and takes the form shown below

$$Q = \frac{-h^2 \Upsilon \underline{\nabla}(\mathrm{M}^{-1}\underline{\nabla}(\mathrm{n}^{\alpha}))}{2\, n^{\alpha}} \tag{2.6}$$

where, $\Upsilon$and α are two adjustable parameters, M^{-1} is the inverse effective mass tensor and n is the electron(or hole) density.

The bohm quantum potential (BQP) model can also be used for the energy balance and hydrodynamic models, where semi classical potential is a modification of the quantum potential in the same way as it is for the continuity equations.

Solving the non linear BQP equation along with a set of semi classical equation uses the iterative scheme as follows. When the initial semi classical solution has been obtained, the BQP equation is solved on its own Gummel iteration to describe Q at every node in the device. Semi-classical potential is then modified by the value of Q at every node and then the set of semi-classical equations is solved for convergence as usual, most probably using a Newton or Block iterative scheme. Then, again the BQP equation is solved to convergence and the process is repeated until self-consistency is gained between the solution of the BQP equation and the set of semi classical equations.

2.4 Models

In our simulation we used following models

models bqp.n bqp.ngamma=1.2 bqp.nalpha=0.5 bqp.p bqp.pgamma=1.0 bqp.palpha=0.5 srh fermi ni.fermi fldmob hcte evsatmod=0

BQP.N specifies the electrons only. The parameters γ_n and α_n used in our simulation are standard against experimental results for silicon.

SRH is Shockley-Read-Hall model. We used *SRH* model in our input deck for carrier generation and recombination for our silicon DG MOSFET device simulation. The mathematical model of Shockley-Read-Hall recombination is as follows,

$$R_{srh} = \frac{pn - n_{ie}^2}{TAUPO\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + TAUNO\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (2.7)$$

where, *ETRAP* is the difference between the trap energy level and the intrinsic fermi level. TAUNO is the electron lifetime and TAUPO is the hole life time. TAUPO and TAUNO are user definable parameter but default value of TAUPO and TAUNO parameters are given in Table 2.1 which we used.

Table 2.1: Default value of the parameter for equation (2.7)

Statement	Parameter	Default	Units
METERIAL	ETRAP	0	eV
METERIAL	TAUNO	1.0×10-7	S
METERIAL	TAUPO	1.0×10-7	S

The electron and hole lifetimes τ_n and τ_P are dependent on concentration. The constant carrier lifetimes are used to make a function of impurity concentration using the following equation

$$R_{srh} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \tau_n\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (2.8)$$

where,

$$\tau_n = \frac{TAUNO}{1 + \frac{N}{NSRHN}} \quad (2.9)$$

$$\tau_P = \frac{TAUPO}{1 + \frac{N}{NSRHP}} \quad (2.10)$$

Here N is the local impurity concentration. The parameters TAUN0, TAUP0, NSRHN and NSRHP have default value shown in Table 2.2

Table 2.2: Default value of the parameter for equation (2.8) to (2.10)

Statement	Parameter	Default	Units
METERIAL	TAUNO	1.0×10-7	S
METERIAL	NSRHN	5.0×1016	cm-3
METERIAL	TAUPO	1.0×10-7	S
METERIAL	NSRHP	5.0×1016	cm-3

For this simulation, we used Fermi-Dirac statistics by using statement **FERMI** in our input deck that gives the probability distribution, f(E) as

$$f(\varepsilon) = \frac{1}{1+\exp\left(\frac{\varepsilon - \mathrm{E_F}}{\kappa \mathrm{T_L}}\right)} \tag{2.11}$$

where, $f(\varepsilon)$ is called Fermi-Dirac probability function, E_F is fermi energy level which is spatially dependant and κ is Boltzmann’s constant.

NI.FERMI use for intrinsic concentration calculation in expressions of SRH recombination and it’s includes the effects of Fermi statistics.

The concentration of electrons and holes can be expressed in terms of the intrinsic carrier concentration as

$$n = n_{ie} \exp[\frac{q(\psi - \varphi_p)}{\kappa \mathrm{T_L}}] \tag{2.12}$$

$$p = n_{ie} \exp \frac{q(\psi - \varphi_p)}{\kappa \mathrm{T_L}}] \tag{2.13}$$

where ψ is the intrinsic potential and φ is the potential corresponding to the fermi level (i.e., $E_F = -q\varphi$).

FLDMOB turns on the parallel electric field-dependent mobility model. For a significant electric field carriers are started to accelerate in that electric field and their velocity will begin to saturate. This phenomenon is responsible for a reduction of the effective mobility since the magnitude of the drift velocity is the product of the mobility and the electric field component in the direction of the current flow. The following expressions are used to implement a field-dependent mobility and show the transition between low-field and high field behavior where:

$$\mu_n(E) = \mu_{n0}\left[\frac{1}{1+\left(\frac{\mu_{n0}\ E}{VSATN}\right)^{BETAN}}\right]^{\frac{1}{BETAN}} \quad (2.14)$$

$$\mu_p(E) = \mu_{p0}\left[\frac{1}{1+\left(\frac{\mu_{p0}\ E}{VSATP}\right)^{BETAP}}\right]^{\frac{1}{BETAP}} \quad (2.15)$$

Here, E is the parallel electric field and μ_{n0} and μ_{p0} are the low field electron and hole mobilities respectively. The low field mobility are either set explicitly in the MOBILITY statement or calculated by one of the low field mobility models.

The BETAN and BETAP are user definable parameter but default value of BETAN and BETAP parameters are given in Table 2.3 which we used.

The saturation velocities are calculated by default from the temperature-dependent models [20].

$$\mathrm{VSATN} = \frac{\mathrm{ALPHAN.FLD}}{1+\mathrm{THETAN.FLD}\exp\left(\frac{T_L}{\mathrm{TNOMN.FLD}}\right)} \quad (2.16)$$

$$\mathrm{VSATP} = \frac{\mathrm{ALPHAN.FLD}}{1+\mathrm{THETAP.FLD}\exp\left(\frac{T_L}{\mathrm{TNOMP.FLD}}\right)} \quad (2.17)$$

Table 2.3: User-Definable Parameters in the Field-Dependent Mobility Model

Statement	**Parameter**	**Default**	**Units**
MOBILITY	BETAN	2.0	
MOBILITY	BETAP	1.0	
MOBILITY	VSATN		cm/s
MOBILITY	VSATP		cm/s
MOBILITY	ALPHAN.FLD	$2.4x10^7$	
MOBILITY	ALPHAP.FLD	$2.4x10^7$	
MOBILITY	THETAN.FLD	0.8	
MOBILITY	THETAP.FLD	0.8	
MOBILITY	TNOMN.FLD	600.0	K
MOBILITY	TNOMP.FLD	600.0	K

It can be set to constant values on the MOBILITY statement by using the VSATN and VSATP parameters. In this case, no temperature dependence is implemented. Specifying the FLDMOB parameter on the MODELS statement invokes the field-dependent mobility. FLDMOB should always be specified unless one of the inversion layer mobility models (which incorporate their own dependence on the parallel field) are specified.

HCTE enables the energy balance model for electrons and holes. In Silvaco models if it is specified all six equations, the Poisson equation, two carrier continuity equations, two carrier energy balance equations, and the lattice heat flow equation are solved.

EVSATMOD = 0

In ATLAS for energy balance transport model four different models have been implemented by setting statement EVSATMOD on the MODELS statement. EVSATMOD = 0 implement the default model for silicon based upon the Caughey-Thomas field-dependent mobility model in Equation (2.14). The resultant relationship between the carrier mobility and the carrier temperature is in the forms:

$$\mu_n = \frac{\mu_{n0}}{\left(1 + X_n^{BETAN}\right)^{\frac{1}{BETAN}}} \tag{2.18}$$

$$\mu_p = \frac{\mu_{p0}}{\left(1 + X_p^{BETAP}\right)^{\frac{1}{BETAP}}} \tag{2.19}$$

$$X_n^{BETAN} = \frac{1}{2}\left(\frac{\alpha_n^{BETAN}\,(T_n - T_L)^{BETAN}}{+\sqrt{\alpha_n^{2BETAN}(T_n - T_L)^{2BETAN} - 4\alpha_n^{BETAN}(T_n - T_L)^{BETAN}}}\right) \tag{2.20}$$

$$X_p^{BETAP} = \frac{1}{2}\left(\frac{\alpha_p^{BETAP}\,(T_n - T_L)^{BETAP}}{+\sqrt{\alpha_n^{2BETAP}\left(T_p - T_L\right)^{2BETAP} - 4\alpha_p^{BETAP}\left(T_p - T_L\right)^{BETAP}}}\right) \tag{2.21}$$

where,

$$\alpha_n = \frac{3}{2}\,\frac{k_B\mu_{n0}}{qVSATN^2\;TAUREL{\cdot}EL} \tag{2.22}$$

$$\alpha_p = \frac{3}{2}\,\frac{k_B\mu_{p0}}{qVSATP^2\;TAUREL{\cdot}HO} \tag{2.23}$$

where μ_{n0} and μ_{p0} are the low field carrier motilities and VSATN and VSATP are the saturated velocities for electrons and holes. The VSATN, VSATP, BETAN, and BETAP parameters are user-definable in the MOBILITY statement. The terms, TAUREL.EL and TAUREL.HO, are the energy relaxation times for electrons and holes and can be defined in the MATERIAL statement.

2.5 Methods

METHOD statement is used to set the numerical methods for successful solutions. All structure and model definitions should precede the METHOD statement and all biasing conditions should follow it. Parameters in the METHOD statement are used to set the solution technique, specify options for each technique and tolerances for convergence.

In out thesis work we have used below method

method climit=1.0e-4 block clim.eb=1.0E7 meinr

CLIMIT = 1.0E-4

Measure of error is provided by the size of the calculated corrections for each unknown. Since the updates are the unknown “xs” at each step, this is called the X norm. Potential updates are measured in units of kT/q. Updates to carrier concentrations are measured relative to the previous value at the point. A value of CLIMIT = 1e-4 is recommended for all simulations of breakdown, where the pre-breakdown current is small.

BLOCK

This method is used for energy balance transport model for iteration process rather than using NEWTON or GUMMEL.

CLIM.EB

It regulates the cut-off carrier concentration below which the program will not consider the error in the carrier temperature. This is applied in energy balance transport model simulations to avoid excessive calculations of the carrier temperature where the carrier concentration is low. But if this parameter is set to very high, where the carrier temperature errors for significant carrier concentrations are being ignored, unpredictable and mostly incorrect results will be experienced.

MEINR

The Meinerzhagens method specifies by using this command, whereby carrier temperature equations will be coupled with the associated carrier continuity equation and used during GUMMEL iterations.

Chapter 3

Results and Discussion

3.1 Structure overview

To perform our work we use Atlas platform of Silvaco as a simulation tool and we obtained the characteristics data of double gate silicon MOSFET for studying scaling effect, body thickness effect, and oxide thickness effect. The 2-dimentational cross section of the device structure obtained from Tony plot tool of Silvaco is shown in Fig. 3.1.

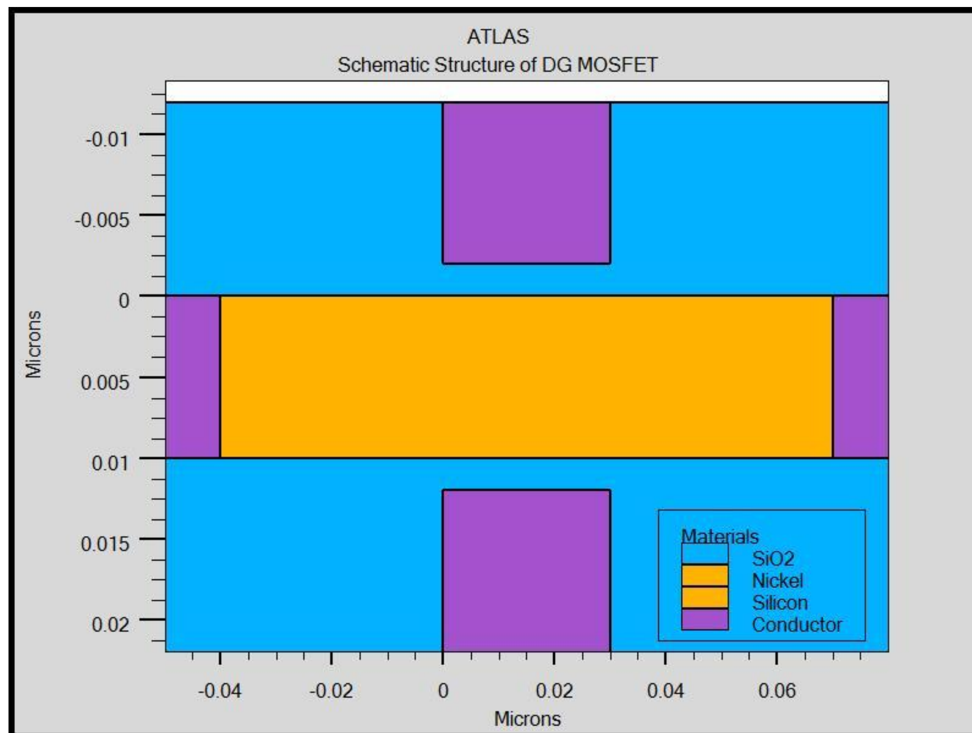

Figure 3.1: Schematic structure of double gate silicon MOSFET.

The structure has two symmetrical gates on its top and bottom. On source and drain we used silicon (Si) with a concentration of $1 \times 10^{19} cm^{-3}$. Silicon dioxide (SiO_2) is used as oxide with a thickness of 2 nm in between gate and body. On gate we used nickel (Ni) as gate electrode to

apply voltage. The work function of Ni is set to 5.25 eV. The silicon body under the gate is undoped.

3.2 Region specification

Different regions parameters of our schematic structure which is shown in Fig. 3.1 are listed below in Table 3.1

Table 3.1: Dimension of different regions of our DG MOSFET structure for Fig. 3.1

Parameter Name	Nominal Value (nm)
Channel length (L_G)	30
Drain length (L_D)	40
Source length (L_S)	40
Body thickness (T_{Body})	10
Electrode thickness (T_{Metal})	10
Oxide thickness (T_{Oxide})	2

The above values are for our initial work. Throughout our research work we are going to modify the channel length, body thickness, and oxide thickness and we will analyze their effects on device performance. In our simulation we apply drain to source voltage V_{DS} = 0.6 V and swing gate bias from -1 V to 3 V.

3.3 Transfer characteristics curve of the double gate Si MOSFET

The I_D-V_{GS} curve of our double gate Si MOSFET with different dimension mentioned in Table 1 is shown in Fig. 3.2. The drain and source doping is $1 \times 10^{19} cm^{-3}$ and the body is undoped. The simulation uses Bohm potential quantum models. The current increases almost exponentially (linear in log scale) and then saturates. The saturation current at V_{GS} = 3V is 3.90 mA/μm for L_G

= 30 nm. The threshold voltage obtains from linear extrapolation of the I_D-V_{GS} shown in Fig. 3.3 is 0.93 V.

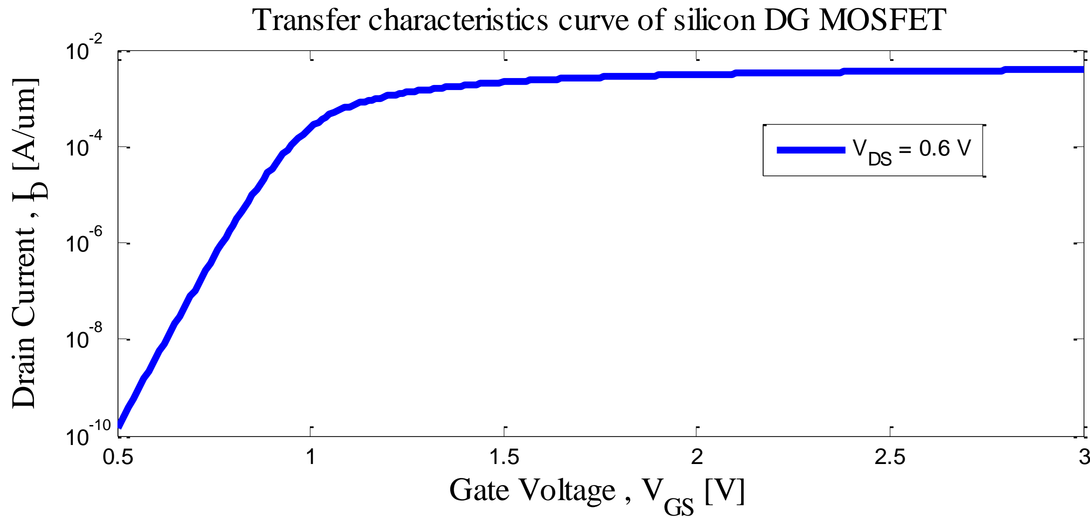

Figure 3.2: I_D vs. V_{GS} characteristics curve of DGMOS with channel length 30 nm in log scale.

3.4 Threshold voltage extraction

The threshold voltage is the minimum gate-to-source voltage which ensures to create a path for electrons movement from source to drain.

Figure 3.3 shows the way we extract threshold voltages for different circumstances, for example, different channel length ranging from (10-100) nm, different body thickness ranging from (5-20) nm, and different oxide thickness ranging from (2-10) nm.

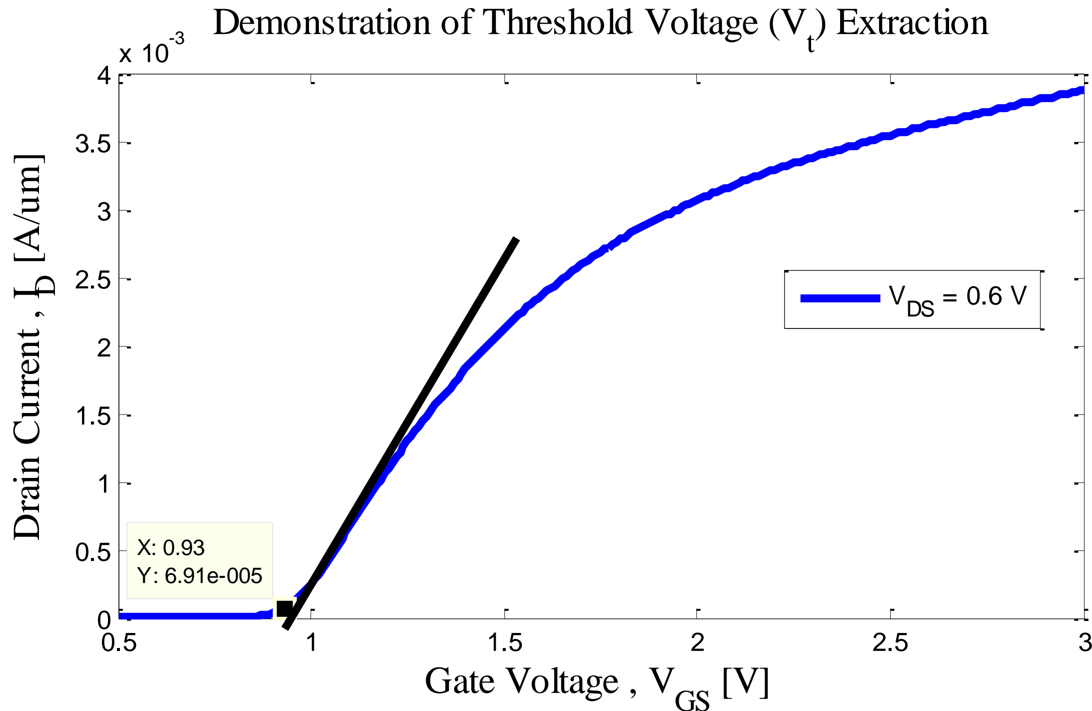

Figure 3.3: Plot for the explanation of how we have extracted threshold voltage. Here the channel length L_G = 30 nm, T_{Body} = 10 nm, T_{Oxide} = 2 nm.

As we got some trouble during threshold voltage extraction from Silvaco using extract command on Silvaco, we plot I_D vs V_{GS} curve on MATLAB. We know that the threshold voltage is a voltage when the MOSFET is just turned on, and with a further increase in gate voltage drive a large amount of drain current. In linear region of I_D vs. V_{GS} curve, we drawn a line and extracted V_t from the intercept of the line to the X-axis.

3.5 Energy Band diagram

In solid-state physics of semiconductor materials, band diagram defines various energy level (i.e. fermi level, conduction level, valance level and nearby energy band edge) on the basis of some spatial dimension. These diagrams offer to describe the operation of different kinds of semiconductor devices and to visualize their band bending. Mainly these band diagrams are modulated by the applied gate voltage and they show the different band bending on different applied gate voltage. It creates channel to flow electrons when the band offers no barrier.

Figure 3.4 shows the conduction band diagram when the applied gate voltage is below threshold ($V_{GS} - V_t = -0.2$ V) and this band diagram still shows some barrier to flow electrons, and the consequence is that the electrons are unable to flow easily form source to drain. This conduction profile is along the channel at the middle of the silicon body (T_{Si} / 2). The channel length here is 30 nm and other dimensions are as per Table 3.1

Conduction energy band below threshold voltage ($V_{GS} - V_t = -0.2$ V)

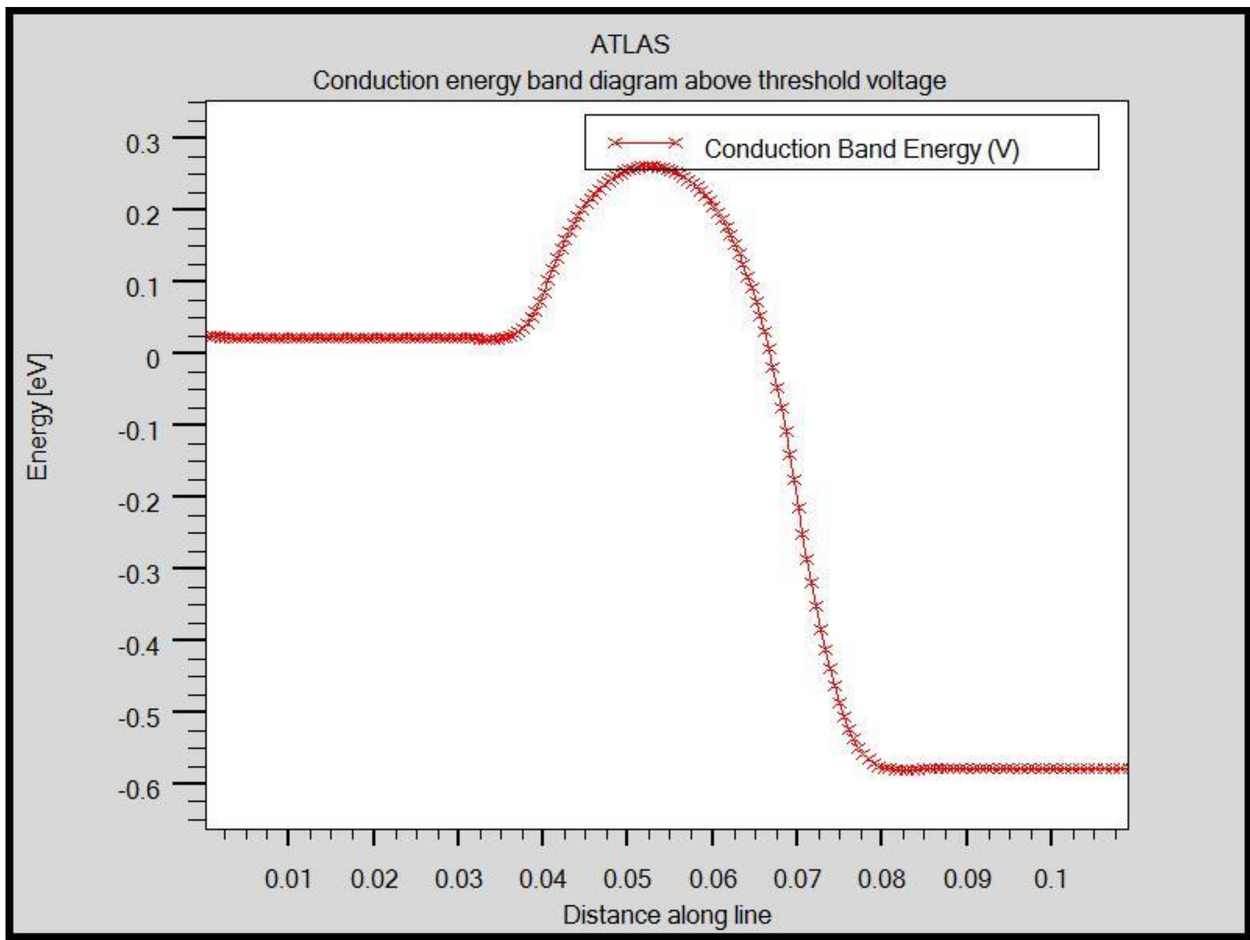

Figure 3.4: Conduction energy band diagram at below threshold. Here L_G = 30 nm, T_{Body} = 10 nm, T_{Oxide} = 2 nm.

Conduction energy band above threshold ($V_{GS} - V_t = 0.6$ V)

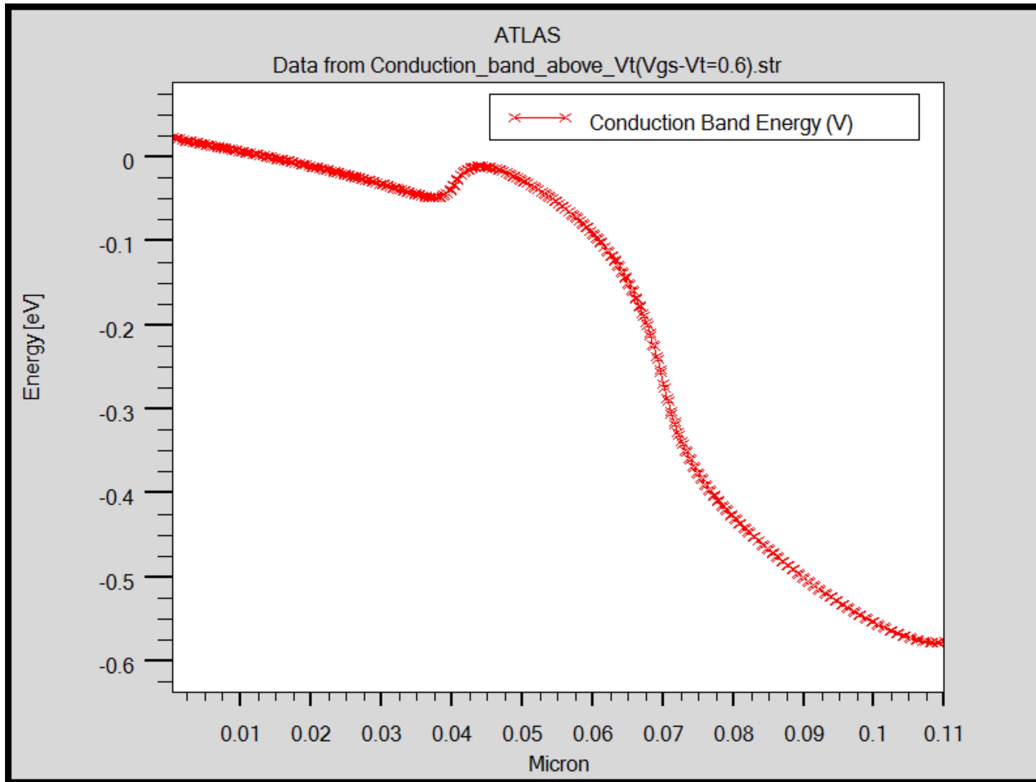

Figure 3.5: Conduction energy band diagram above threshold. Here $L_G = 30$ nm, $T_{Body} = 10$ nm, $T_{Oxide} = 2$ nm.

Figure 3.5 shows conduction energy band diagram when the applied gate voltage is ($V_{GS} - V_t = 0.6$ V). As the gate voltage increases barrier is lowering. When the applied gate voltage is above threshold the barrier is removed. As a result electrons can flow from source to drain without facing the barrier.

3.6 Scaling of gate length

In this section we observe the effect of channel length on the I_D-V_{GS} curves, mainly threshold voltage roll-off and saturation current.

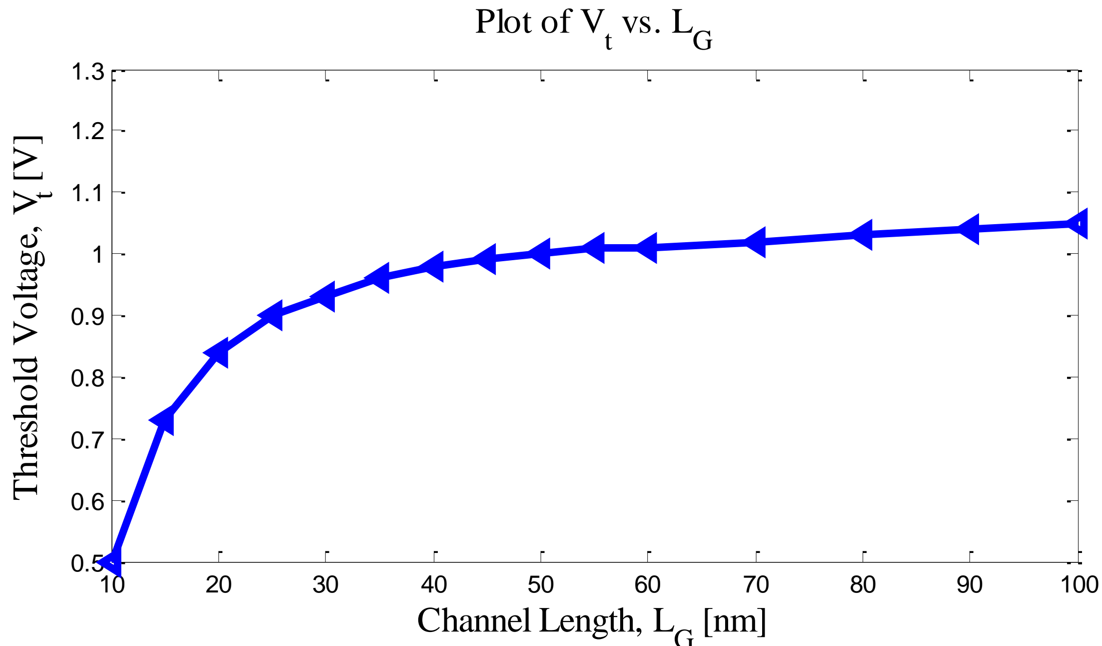

Figure 3.6: Plot of threshold voltage vs. channel length. Here channel length is varied from 10 nm to 100 nm, with T_{Body} = 10 nm, T_{Oxide} = 2 nm. V_{DS} = 0.6 V.

Figure 3.6 shows the threshold voltage vs. channel length. In this figure, all the dimensions as mentioned in Table 3.1 are same except the channel length, L_G. Up to L_G = 40 nm, the V_t is almost constant and below it V_t start to decrease. That is short channel effects start when L_G goes below 40 nm.

Now we observe the sub-threshold slope for different gate length from 10 nm to 100 nm, Sub-threshold slope is amount of gate voltage required to raise one decade of drain current in sub-threshold region. There is a small change in sub-threshold slope in the long channel region, sub-threshold slope is 66.91 mV/decade to 61.39 mV/decade where channel length is 40 nm to 100

nm. But in the short channel region change in sub-threshold slope is significant, sub-threshold slope is changing from 113.8 mV/decade to 66.91 mV/decade when channel length changes from 10 nm to 40 nm.

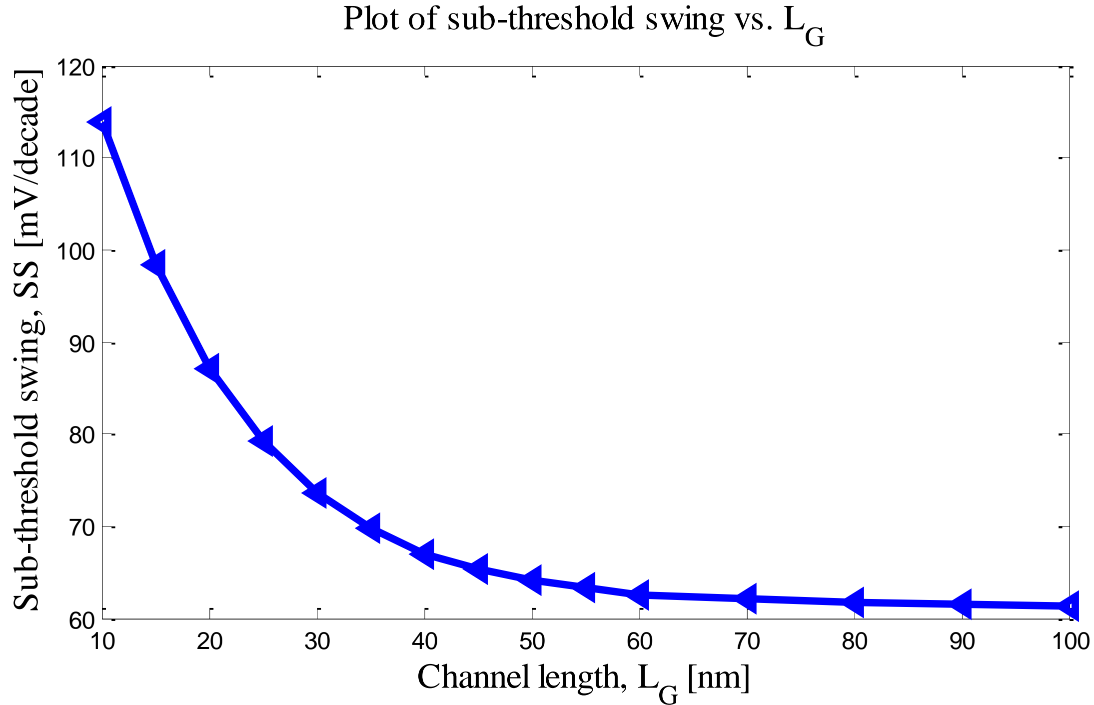

Figure 3.7: Plot of sub-threshold swing vs. channel length.

3.7 DG MOSFET ON Current

Now we observe the ON current for different body thickness of three different channel lengths of Si DG MOSFET. The ON current is defined at $V_{GS} = V_t + V_{DS}$. ON current is increasing with increasing body thickness and decreasing with increasing gate length. At 5 nm body thickness, ON currents are 1.52 mA/µm, 1.45 mA/µm, and 1.32 mA/µm when channel lengths are 20 nm, 40 nm, and 80 nm respectively. And at 20 nm body thickness, ON currents are 2.63 mA/µm, 2.46 mA/µm and 2.02 mA/µm when channel lengths are 20 nm, 40 nm, and 60 nm respectively.

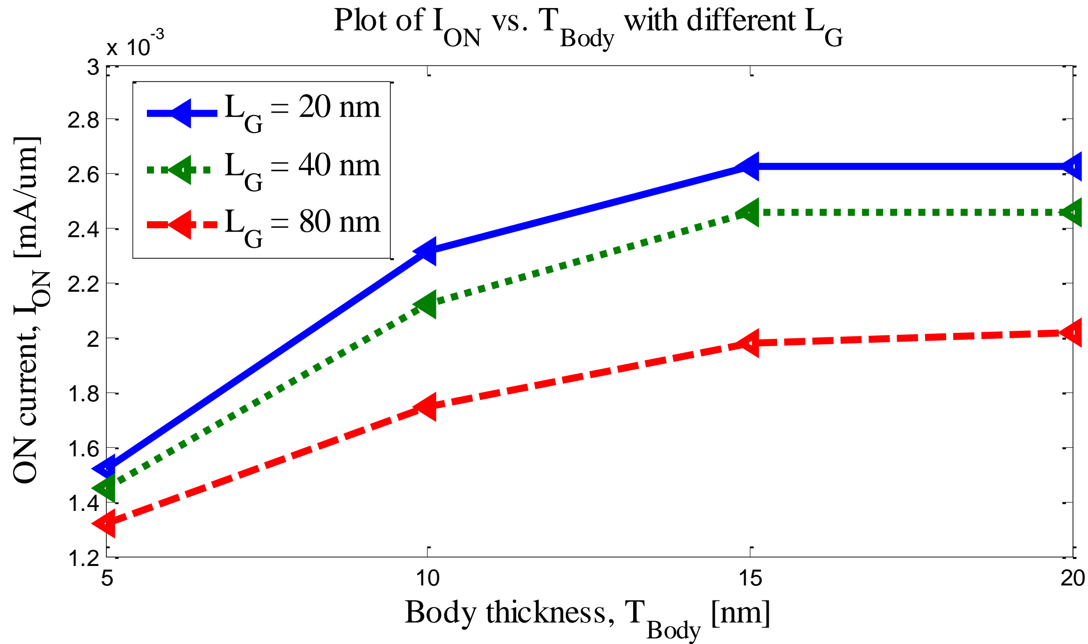

Figure 3.8: Plot of I_{ON} vs. T_{Si} with L_G = 20 nm, 40 nm, 60 nm.

3.8 Body Thickness Effect

Next we observe the effect of silicon body thickness on V_t for 3 different values of L_G, 80 nm (long channel), 40 nm (near long channel and short channel), and 20 nm (short channel). In the long channel or near long channel region, the body thickness effect on the threshold voltage is negligible. However, in the short channel region (L_G ~ 20 nm) the threshold voltage changes significantly with silicon body thickness. The V_t changes from 0.95 V to 0.56 V when T_{Body} changes from 5 nm to 20 nm.

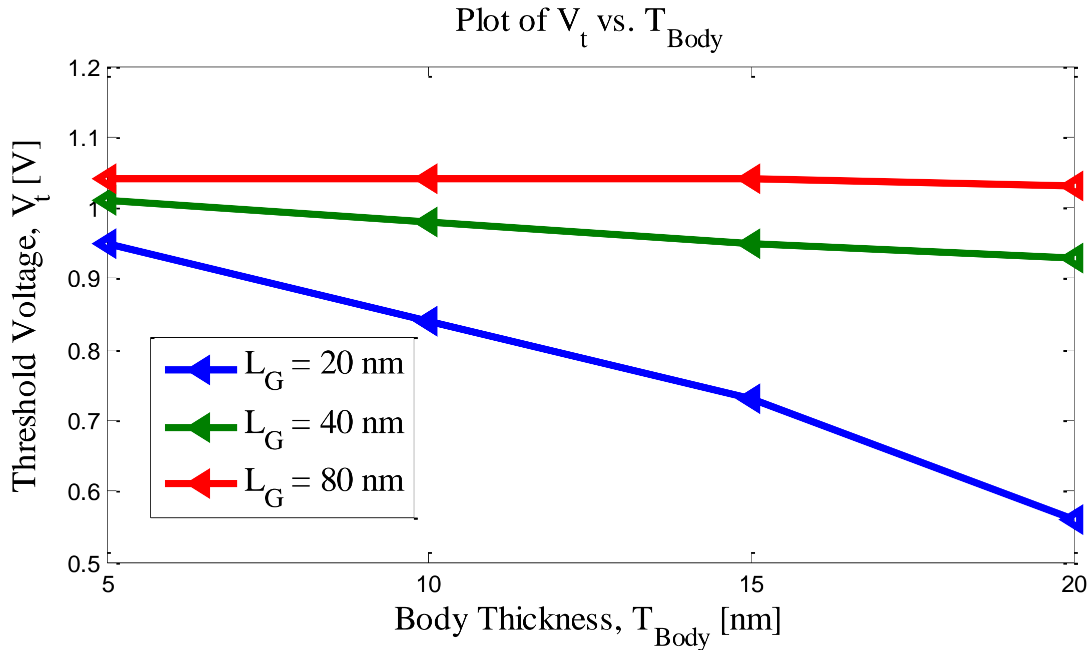

Figure 3.9: Plot of threshold voltage vs. body thickness with L_G = 20 nm, 40 nm, 60 nm.

3.9 Oxide Thickness Effect

Now we observe the effect of silicon-dioxide (SiO_2) thickness on V_t for 3 different values of L_G, 60 nm (long channel), 40 nm (near long channel and short channel), and 20 nm (short channel). In the long channel or close to long channel region, the oxide thickness effect on the threshold voltage is insignificant. However, in the short channel region (L_G ~ 20nm) the threshold voltage changes significantly with oxide thickness. The V_t changes from 0.84 V to 0.16 V when T_{Oxide} changes from 2 nm to 10 nm.

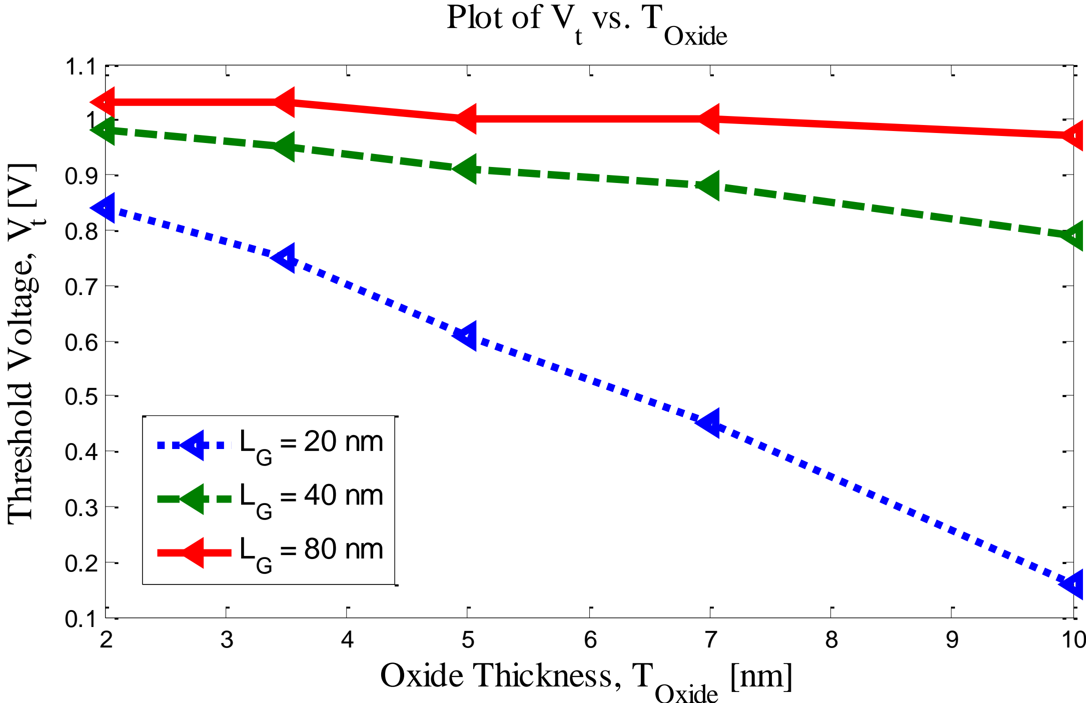

Figure 3.10: Plot of V_t vs. T_{Oxide} with L_G = 20 nm, 40 nm, 60 nm.

Chapter 4

Conclusion

Engineers are scaling down the MOS to obtain higher performance and the consequences are several short channel effects. To achieve the roadmap of high performance MOS, engineers need to suppress those short channel effects. Most common effect is increase in static power dissipation during the off state of the transistor. A number of fundamental limits prevent the traditional scaling of conventional bulk MOSFET's. It becomes necessary to incorporate some innovations in materials or structures to prolong device scaling for technology nodes. Silicon DG MOSFET is a novel structured device which showing much better performance than single gate MOSFET and provide an opportunity to further reduction of channel length. We have studied on channel length modification, gate oxide thickness modification, T_{si} modification. With small dimensions the device performance degrades due to severe short channel effects such as threshold voltage roll off. With a source/drain doping density of$10^{19}\ cm^{-3}$, and SiO_2 thickness of 2 nm, the short channel effects start when the channel length goes below 40 nm. The variation of other dimensions such as oxide thickness and channel body thickness affect the threshold voltage and sub-threshold swing in short channel region.

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